



Politechnika Wrocławska

# Układy scalone analogowe i analogowo - cyfrowe

# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

### LMC 7660 - Switched Capacitor Voltage Converter

(konwerter napięcia z przełączaną pojemnością)

Układ LMC 7660 (z rodziny układów 7660: ICL7660, MAX 1044) jest wykonany w technologii CMOS. Umożliwia on zamianę dodatniego napięcia z zakresu (1.5 - 10) V na odpowiadające mu co do wartości bezwzględnej napięcie ujemne:

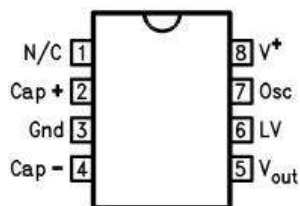
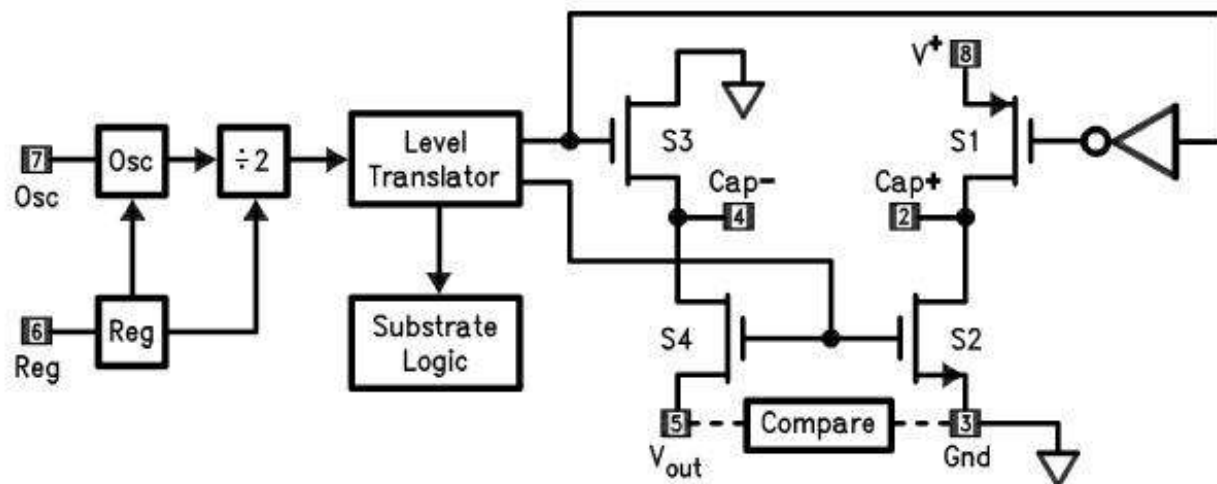
$$U_{OUT} = -U_{IN}$$

$$\text{dla: } U_{IN} = +(1.5 \div 10)V$$

# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

Rys. 1. Schemat blokowy układu



Package	Temperature Range	NSC Drawing
	Industrial -40°C to +85°C	
8-Lead Molded DIP	LMC7660IN	N08E
8-Lead Molded Small Outline	LMC7660IM	M08A

Rys. 2. Obudowa i opis wyprowadzeń

# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

### Główne cechy układu

## Features

- Operation over full temperature and voltage range without an external diode
- Low supply current, 200  $\mu$ A max
- Pin-for-pin replacement for the 7660
- Wide operating range 1.5V to 10V
- 97% Voltage Conversion Efficiency
- 95% Power Conversion Efficiency
- Easy to use, only 2 external components
- Extended temperature range
- Narrow SO-8 Package



# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

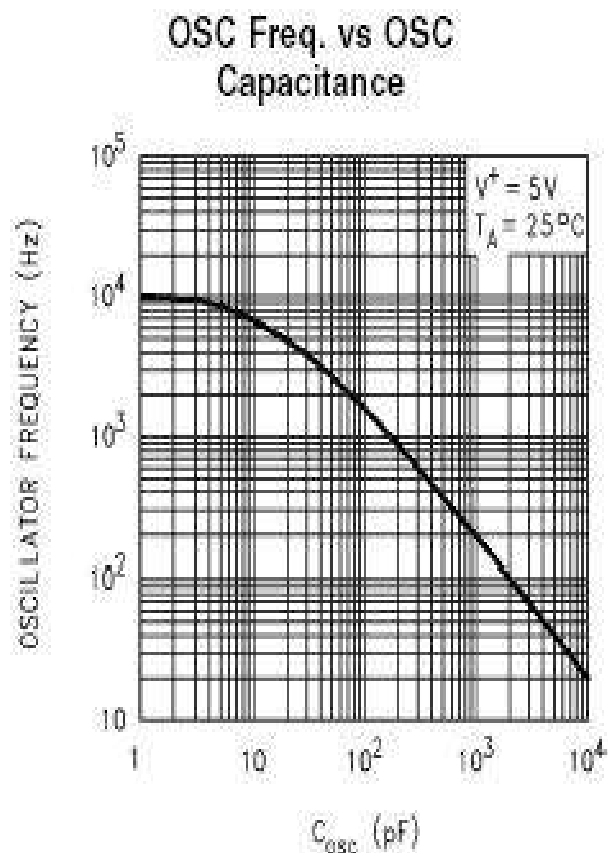
**Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	Typ	LMC7660IN/ LMC7660IM	Units Limits
				Limit (Note 5)	
$I_s$	Supply Current	$R_L = \infty$	120	200 400	$\mu A$ max
$V^+H$	Supply Voltage Range High (Note 6)	$R_L = 10\text{ k}\Omega$ , Pin 6 Open Voltage Efficiency $\geq 90\%$	3 to 10	3 to 10 3 to 10	V
$V^+L$	Supply Voltage Range Low	$R_L = 10\text{ k}\Omega$ , Pin 6 to Gnd. Voltage Efficiency $\geq 90\%$	1.5 to 3.5	1.5 to 3.5 1.5 to 3.5	V
$R_{out}$	Output Source Resistance	$I_L = 20\text{ mA}$	55	100 120	$\Omega$ max
		$V = 2V$ , $I_L = 3\text{ mA}$ Pin 6 Short to Gnd.	110	200 300	$\Omega$ max
$F_{osc}$	Oscillator Frequency		10		kHz
$P_{eff}$	Power Efficiency	$R_L = 5\text{ k}\Omega$	97	95 90	% min
$V_{o\ off}$	Voltage Conversion Efficiency	$R_L = \infty$	99.9	97 95	% min
$I_{osc}$	Oscillator Sink or Source Current	Pin 7 = Gnd. or $V^+$	3		$\mu A$

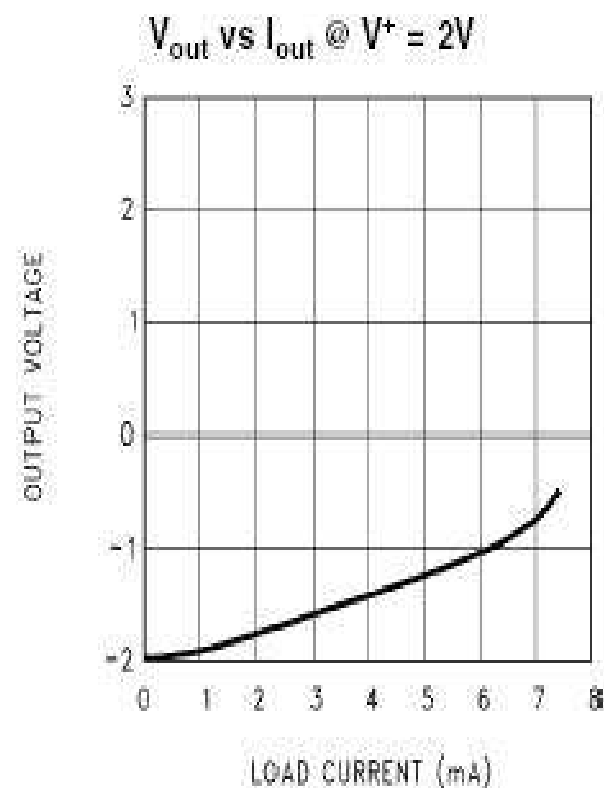
# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

### Typical Performance Characteristics



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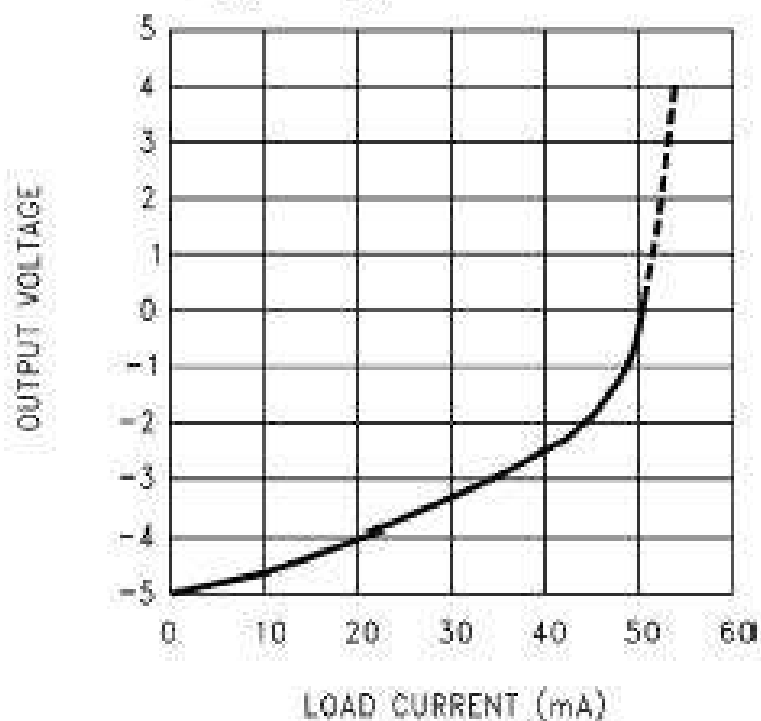


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# Układy zasilające - rodzina 7660

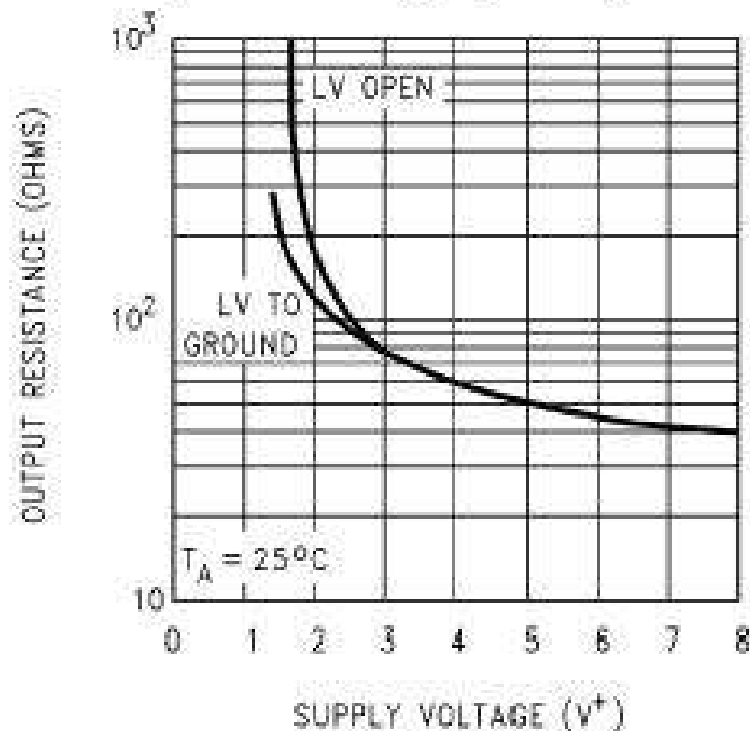
## LMC 7660 - National Semiconductor

$V_{out}$  vs  $I_{out}$  @  $V^+ = 5V$



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Output R vs Supply Voltage

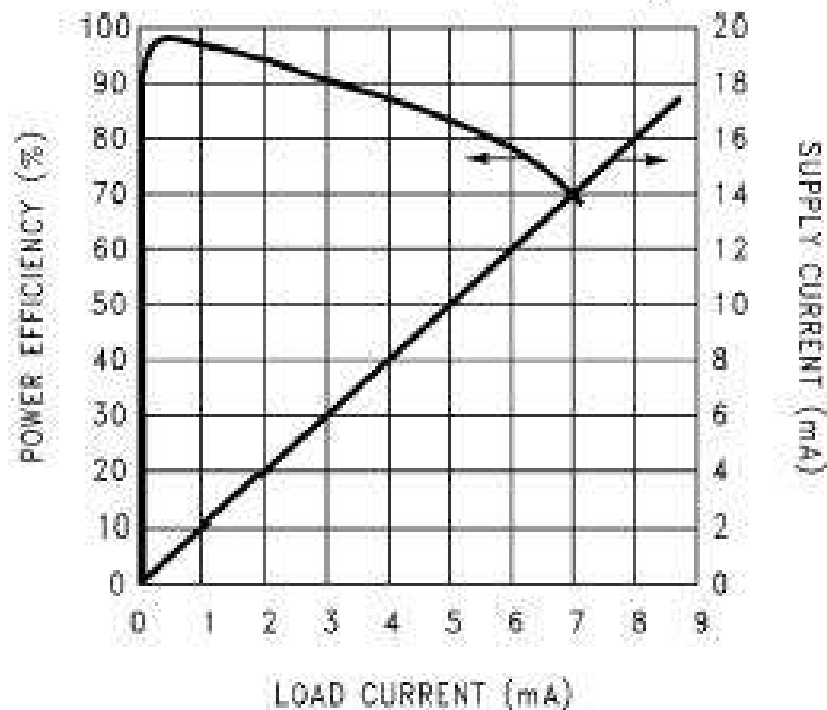




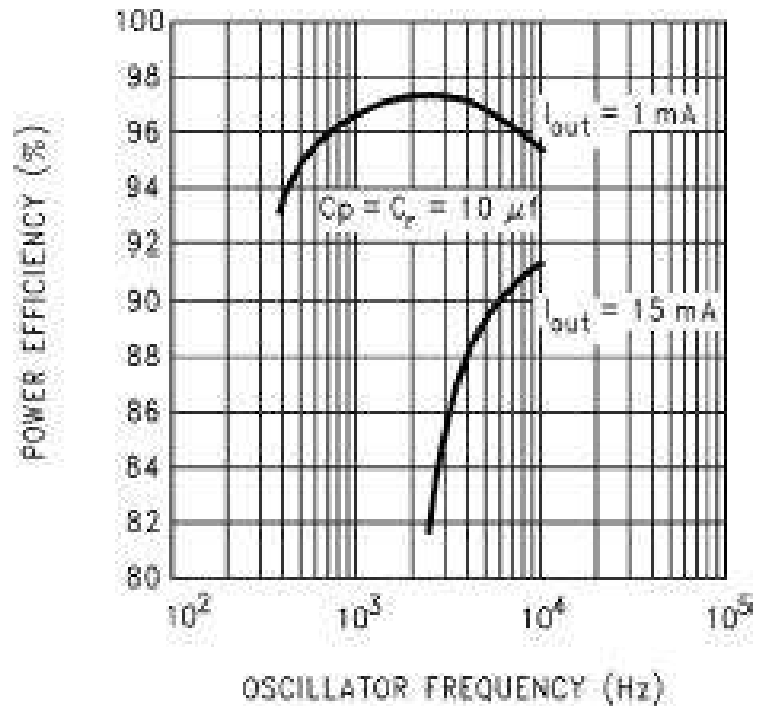
# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor

Supply Current & Power Efficiency  
vs Load Current ( $V^+ = 2V$ )



$P_{eff}$  vs OSC Freq. @  $V^+ = 5V$







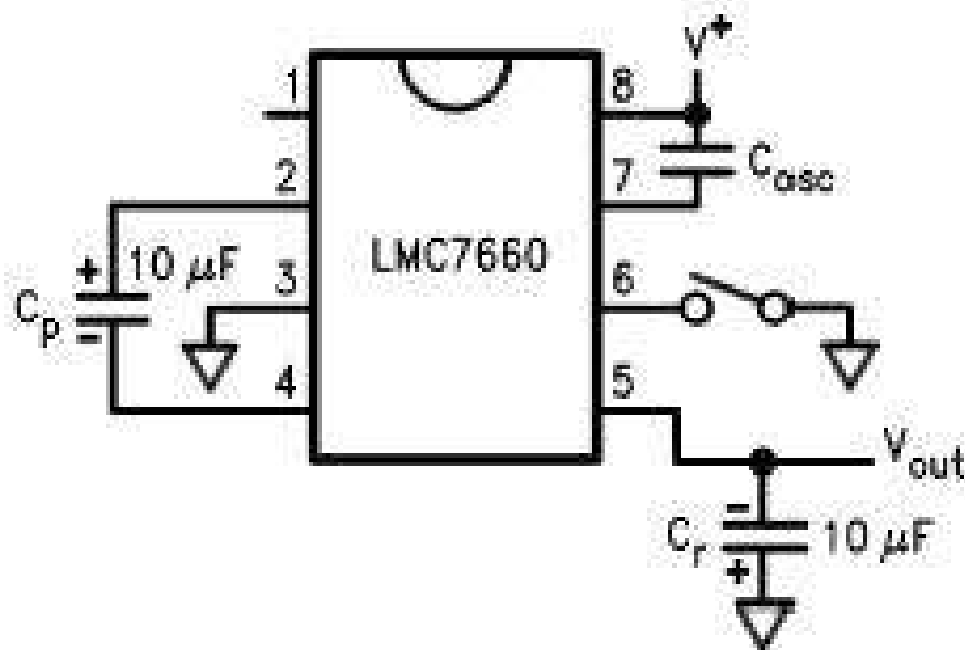
## Układy zasilające - rodzina 7660 LMC 7660 - National Semiconductor

Oprócz wymienionych informacji producent podaje:

- sposób obniżenia prądu pobieranego przez układ - zmniejszenie częstotliwości pracy
- sposób synchronizacji układu z zewnętrznym zegarem/oscylatorem
- sposób obniżenia impedancji wyjściowej konwertera

# Układy zasilające - rodzina 7660

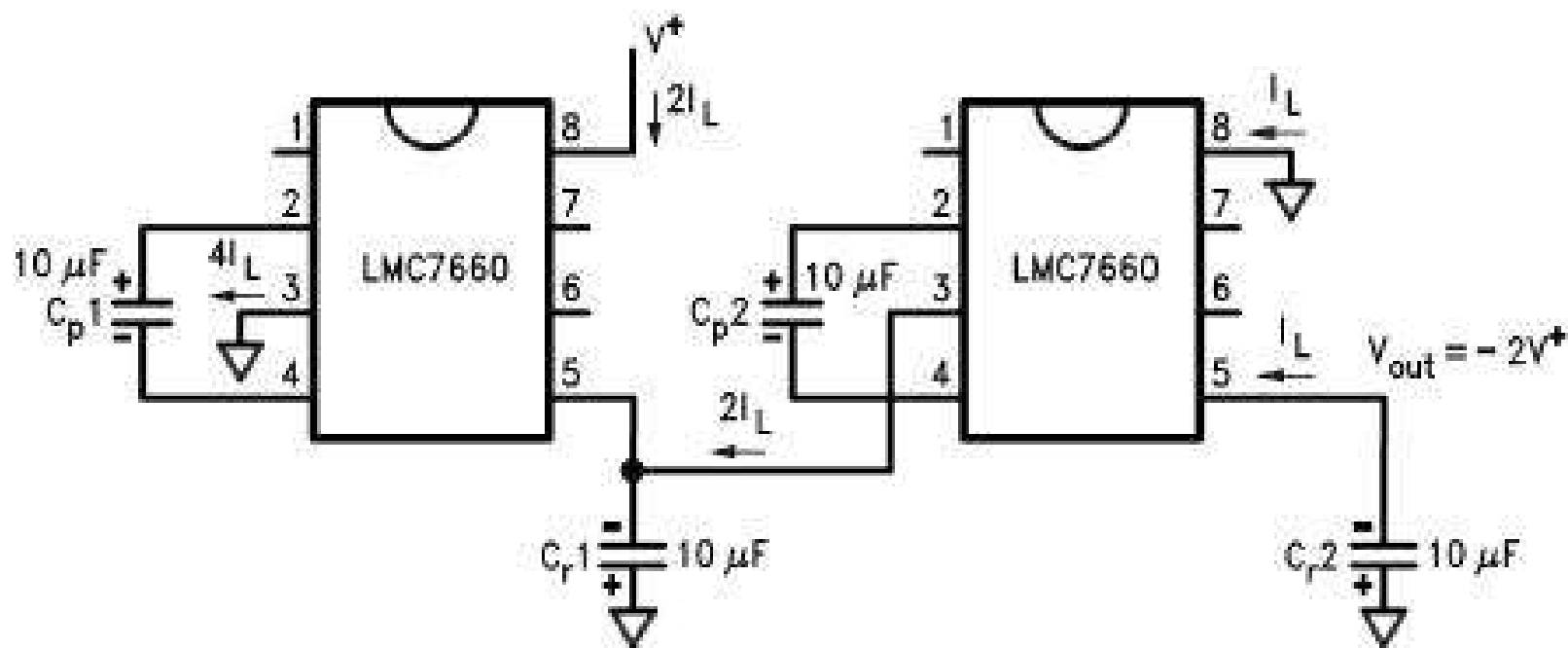
## LMC 7660 - National Semiconductor



Rys. 3. Schemat podstawowej aplikacji układu LMC 7660

# Układy zasilające - rodzina 7660

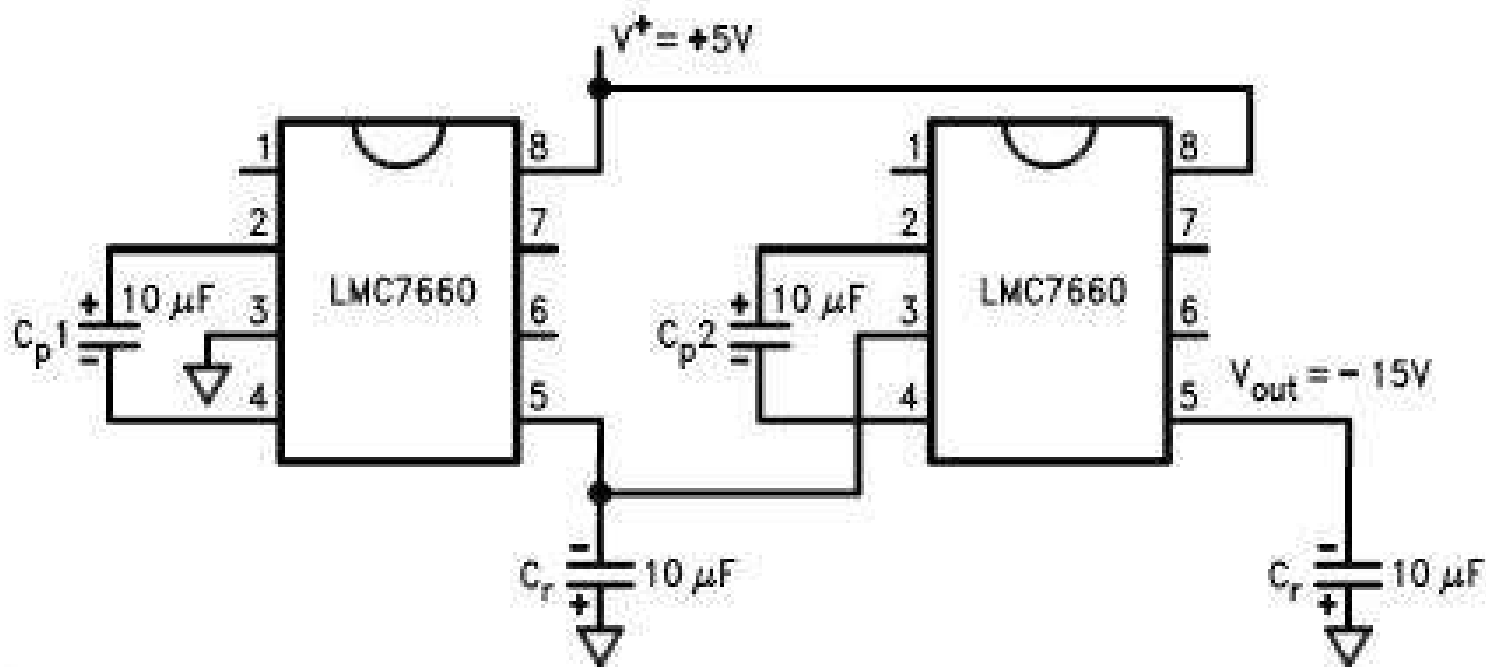
## LMC 7660 - National Semiconductor



Rys. 4. Układ o podwojonej wartości napięcia  
wyjściowego

# Układy zasilające - rodzina 7660

## LMC 7660 - National Semiconductor



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Rys. 5. Potrajacz napięcia

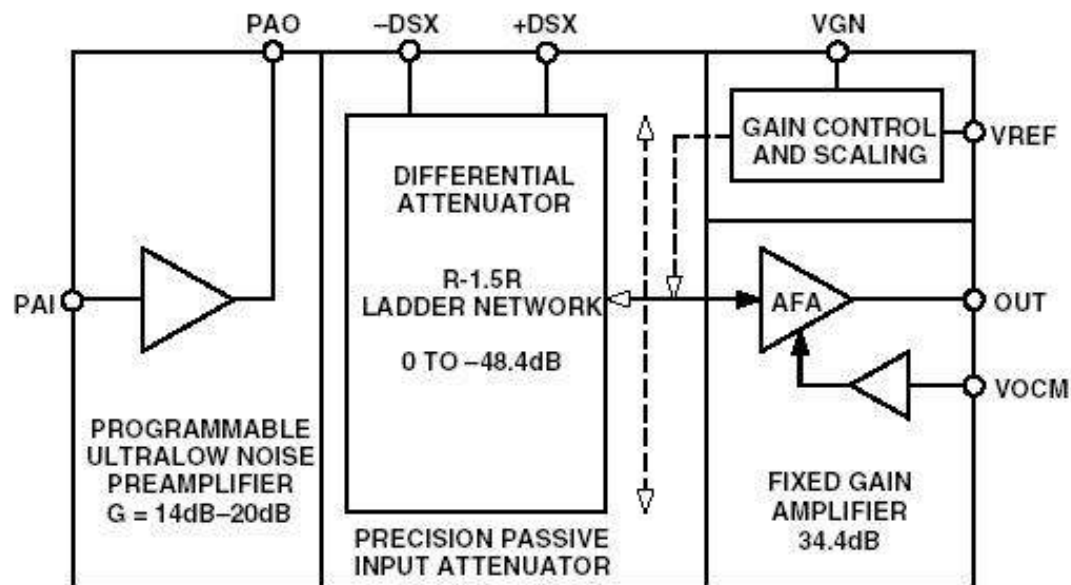
# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

**AD 604** - dual, ultralow noise, variable gain Amplifier

Układ AD 604 jest podwójnym, niskoszumnym wzmacniaczem operacyjnym o regulowanym wzmacnieniu.

FUNCTIONAL BLOCK DIAGRAM





# **Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu**

## **AD 604 - Analog Devices**

### **FEATURES**

**Ultralow Input Noise at Maximum Gain:**

**$0.80 \text{ nV}/\sqrt{\text{Hz}}$ ,  $3.0 \text{ pA}/\sqrt{\text{Hz}}$**

**2 Independent Linear-in-dB Channels**

**Absolute Gain Range per Channel Programmable:**

**0 dB to 48 dB (Preamp Gain = 14 dB), through**

**6 dB to 54 dB (Preamp Gain = 20 dB)**

**$\pm 1.0$  dB Gain Accuracy**

**Bandwidth: 40 MHz (–3 dB)**

**300 k $\Omega$  Input Resistance**

**Variable Gain Scaling: 20 dB/V through 40 dB/V**

**Stable Gain with Temperature and Supply Variations**

**Single-Ended Unipolar Gain Control**

**Power Shutdown at Lower End of Gain Control**

**Can Drive ADCs Directly**

### **APPLICATIONS**

**Ultrasound and Sonar Time-Gain Control**

**High Performance AGC Systems**

**Signal Measurement**



# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

Producent podaje zależność opisującą wzmacnienie układu w funkcji napięcia sterującego wzmacnieniem:

$$G \text{ (dB)} = \left( \text{Gain Scaling (dB/V)} \times V_{GN} \text{ (V)} \right) + \left( \text{Preamp Gain (dB)} - 19 \text{ dB} \right)$$

gdzie:

$G(\text{dB})$  - wzmacnienie pojedynczego kanału w [dB]

$\text{Gain Scaling (dB/V)}$  - współczynnik skalowania napięcia sterującego wzmacnieniem

$V_{GN}(\text{V})$  - napięcie sterujące wartością wzmacnienia

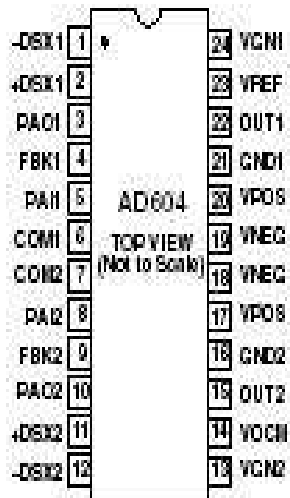
$\text{Preamp Gain (dB)}$  - wzmacnienie przedwzmacniacza [dB]



# Układy wzmacniające - wzmacniacze o regulowanym wzmocnieniu

## AD 604 - Analog Devices

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	-DSX1	CH1 Negative Signal Input to DSX1.
2	+DSX1	CH1 Positive Signal Input to DSX1.
3	PAO1	CH1 Preamplifier Output.
4	FBK1	CH1 Preamplifier Feedback Pin.
5	PAI1	CH1 Preamplifier Positive Input.
6	COM1	CH1 Signal Ground. When connected to positive supply, Preamplifier 1 will shut down.
7	COM2	CH2 Signal Ground. When connected to positive supply, Preamplifier 2 will shut down.
8	PAI2	CH2 Preamplifier Positive Input.
9	FBK2	CH2 Preamplifier Feedback Pin.
10	PAO2	CH2 Preamplifier Output.
11	+DSX2	CH2 Positive Signal Input to DSX2.
12	-DSX2	CH2 Negative Signal Input to DSX2.
13	VGN2	CH2 Gain-Control Input and Power-Down Pin. If grounded, device is off; otherwise, positive voltage increases gain.
14	VOCM	Input to this pin defines the common-mode of the output at OUT1 and OUT2.
15	OUT2	CH2 Signal Output.
16	GND2	Ground.
17	VPOS	Positive Supply.
18	VNEG	Negative Supply.
19	VNEG	Negative Supply.
20	VPOS	Positive Supply.
21	GND1	Ground.
22	OUT1	CH1 Signal Output.
23	VREF	Input to this pin sets gain-scaling for both channels to 2.5 V = 20 dB/V, 1.67 V = 30 dB/V.
24	VGN1	CH1 Gain-Control Input and Power-Down Pin. If grounded, the device is off; otherwise, positive voltage increases gain.





# Układy wzmacniające - wzmacniacze o regulowanym wzmocnieniu

## AD 604 - Analog Devices

Parameter	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>					
Preamplifier					
Input Resistance			300		k $\Omega$
Input Capacitance			8.5		pF
Input Bias Current			-27		$\mu$ A
Peak Input Voltage	Preamp Gain = 14 dB		$\pm 400$		mV
	Preamp Gain = 20 dB		$\pm 200$		mV
Input Voltage Noise	VGN = 2.9 V, $R_S = 0 \Omega$				
	Preamp Gain = 14 dB		0.8		nV/ $\sqrt{Hz}$
	Preamp Gain = 20 dB		0.73		nV/ $\sqrt{Hz}$
Input Current Noise	Independent of Gain		3.0		pA/ $\sqrt{Hz}$
Noise Figure	$R_S = 50 \Omega$ , $f = 10$ MHz, VGN = 2.9 V		2.3		dB
	$R_S = 200 \Omega$ , $f = 10$ MHz, VGN = 2.9 V		1.1		dB
<b>DSX</b>					
Input Resistance			175		$\Omega$
Input Capacitance			3.0		pF
Peak Input Voltage			$2.5 \pm 2$		V
Input Voltage Noise	VGN = 2.9 V		1.8		nV/ $\sqrt{Hz}$
Input Current Noise	VGN = 2.9 V		2.7		pA/ $\sqrt{Hz}$
Noise Figure	$R_S = 50 \Omega$ , $f = 10$ MHz, VGN = 2.9 V		8.4		dB
	$R_S = 200 \Omega$ , $f = 10$ MHz, VGN = 2.9 V		12		dB
Common-Mode Rejection Ratio	$f = 1$ MHz, VGN = 2.65 V		-20		dB



# Układy wzmacniające - wzmacniacze o regulowanym wzmocnieniu

## AD 604 - Analog Devices

OUTPUT CHARACTERISTICS			
-3 dB Bandwidth	Constant with Gain	40	MHz
Slew Rate	V <sub>GN</sub> = 1.5 V, Output = 1 V Step	170	V/μs
Output Signal Range	R <sub>L</sub> ≥ 500 Ω	2.5 ± 1.5	V
Output Impedance	f = 10 MHz	2	Ω
Output Short-Circuit Current		±40	mA
Harmonic Distortion	V <sub>GN</sub> = 1 V, V <sub>OUT</sub> = 1 V p-p		
HD2	f = 1 MHz	-54	dBc
HD3	f = 1 MHz	-67	dBc
HD2	f = 10 MHz	-43	dBc
HD3	f = 10 MHz	-48	dBc
Two-Tone Intermodulation Distortion (IMD)	V <sub>GN</sub> = 2.9 V, V <sub>OUT</sub> = 1 V p-p		
	f = 1 MHz	-74	dBc
	f = 10 MHz	-71	dBc
Third-Order Intercept	f = 10 MHz, V <sub>GN</sub> = 2.65 V, V <sub>OUT</sub> = 1 V p-p, Input Referred	-12.5	dBm
1 dB Compression Point	f = 1 MHz, V <sub>GN</sub> = 2.9 V, Output Referred	15	dBm
Channel-to-Channel Crosstalk	V <sub>OUT</sub> = 1 V p-p, f = 1 MHz		
	Ch No. 1: V <sub>GN</sub> = 2.65 V, Inputs Shorted	-30	dB
	Ch No. 2: V <sub>GN</sub> = 1.5 V (Mid Gain)		dB
Group Delay Variation	1 MHz < f < 10 MHz, Full Gain Range	±2	ns
VOCM Input Resistance		45	kΩ



# Układy wzmacniające - wzmacniacze o regulowanym wzmocnieniu

## AD 604 - Analog Devices

ACCURACY					
Absolute Gain Error					
0 dB to 3 dB	$0.25\text{ V} < V_{GN} < 0.400\text{ V}$	-1.2	+0.75	+3	dB
3 dB to 43 dB	$0.400\text{ V} < V_{GN} < 2.400\text{ V}$	-1.0	$\pm 0.3$	+1.0	dB
43 dB to 48 dB	$2.400\text{ V} < V_{GN} < 2.65\text{ V}$	-3.5	-1.25	+1.2	dB
Gain Scaling Error	$0.400\text{ V} < V_{GN} < 2.400\text{ V}$		$\pm 0.25$		dB/V
Output Offset Voltage	$V_{REF} = 2.500\text{ V}, V_{OCM} = 2.500\text{ V}$	-50	$\pm 30$	+50	mV
Output Offset Variation	$V_{REF} = 2.500\text{ V}, V_{OCM} = 2.500\text{ V}$		30	50	mV



# Układy wzmacniające - wzmacniacze o regulowanym wzmocnieniu

## AD 604 - Analog Devices

Parameter	Conditions	Min	Typ	Max	Unit
<b>GAIN CONTROL INTERFACE</b>					
Gain Scaling Factor	$V_{REF} = 2.5 \text{ V}$ , $0.4 \text{ V} < V_{GN} < 2.4 \text{ V}$	19	20	21	dB/V
Gain Range	$V_{REF} = 1.67 \text{ V}$		30		dB/V
	Preamp Gain = 14 dB		0 to 48		dB
	Preamp Gain = 20 dB		6 to 54		dB
Input Voltage ( $V_{GN}$ ) Range	20 dB/V, $V_{REF} = 2.5 \text{ V}$		0.1 to 2.9		V
Input Bias Current			-0.4		$\mu\text{A}$
Input Resistance			2		M $\Omega$
Response Time	48 dB Gain Change		0.2		$\mu\text{s}$
$V_{REF}$ Input Resistance			10		k $\Omega$
<b>POWER SUPPLY</b>					
Specified Operating Range	One Complete Channel		$\pm 5$		V
	One DSX Only		5		V
Power Dissipation	One Complete Channel		220		mW
	One DSX Only		95		mW
Quiescent Supply Current	$V_{POS}$ , One Complete Channel		32	36	mA
	$V_{POS}$ , One DSX Only		19	23	mA
	$V_{NEG}$ , One Preamplifier Only	-15	-12		mA
Powered Down	$V_{POS}$ , $V_{GN} < 50 \text{ mV}$ , One Channel		1.9	3.0	mA
	$V_{NEG}$ , $V_{GN} < 50 \text{ mV}$ , One Channel		-150		$\mu\text{A}$
Power-Up Response Time	48 dB Gain Change, $V_{OUT} = 2 \text{ V p-p}$		0.6		$\mu\text{s}$
Power-Down Response Time			0.4		$\mu\text{s}$

# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

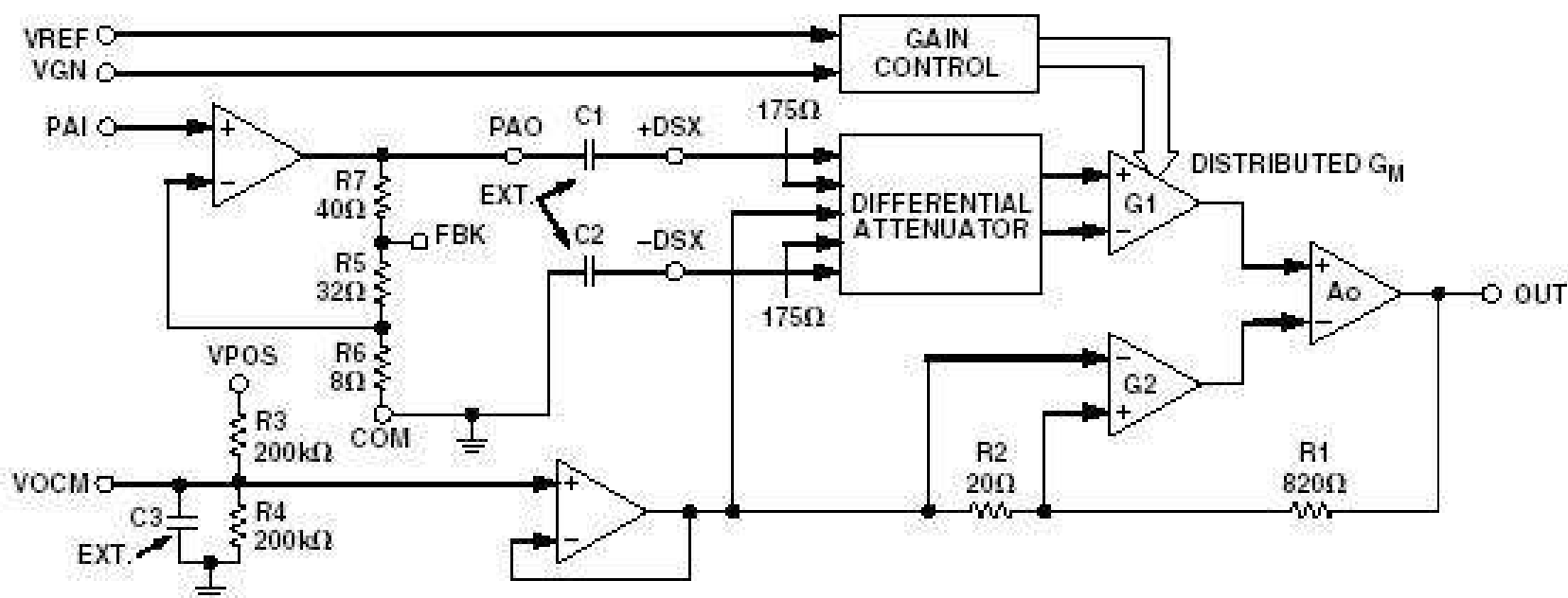


Figure 35. Simplified Block Diagram of a Single Channel of the AD604

# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

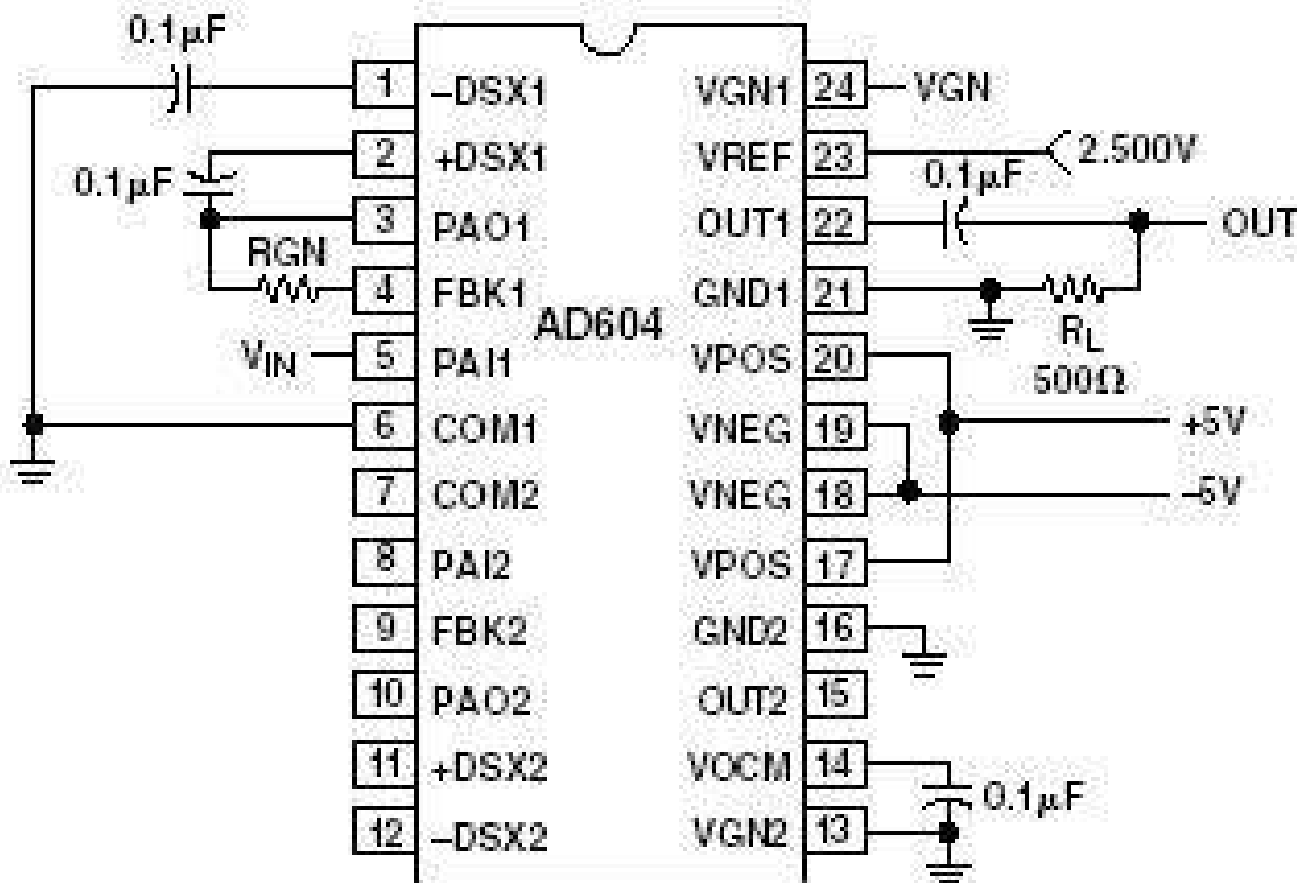


Figure 41. Basic Connections for a Single Channel

# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

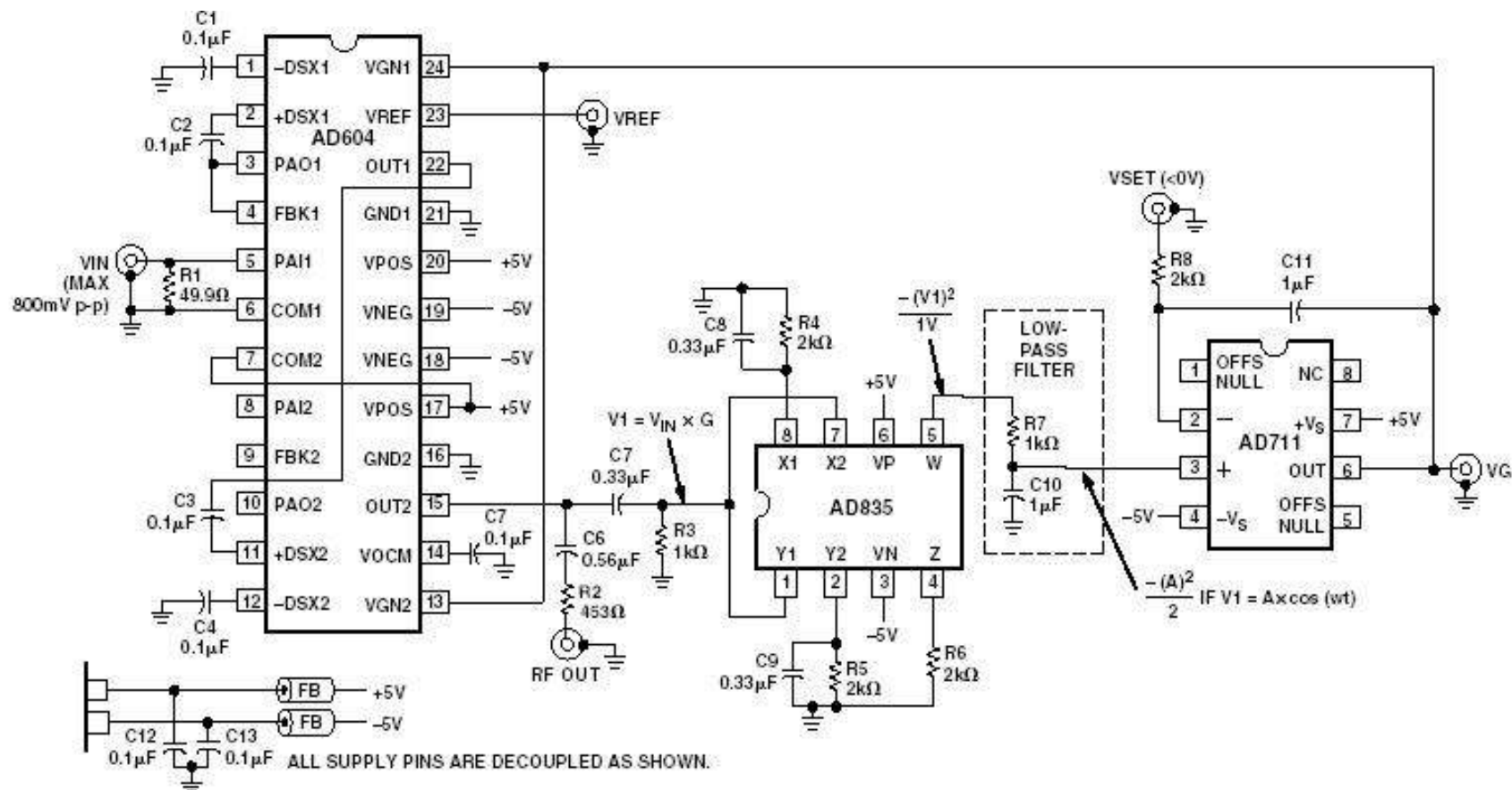


Figure 42. AGC Amplifier with 82 dB of Gain Range

# Układy wzmacniające - wzmacniacze o regulowanym wzmacnieniu

## AD 604 - Analog Devices

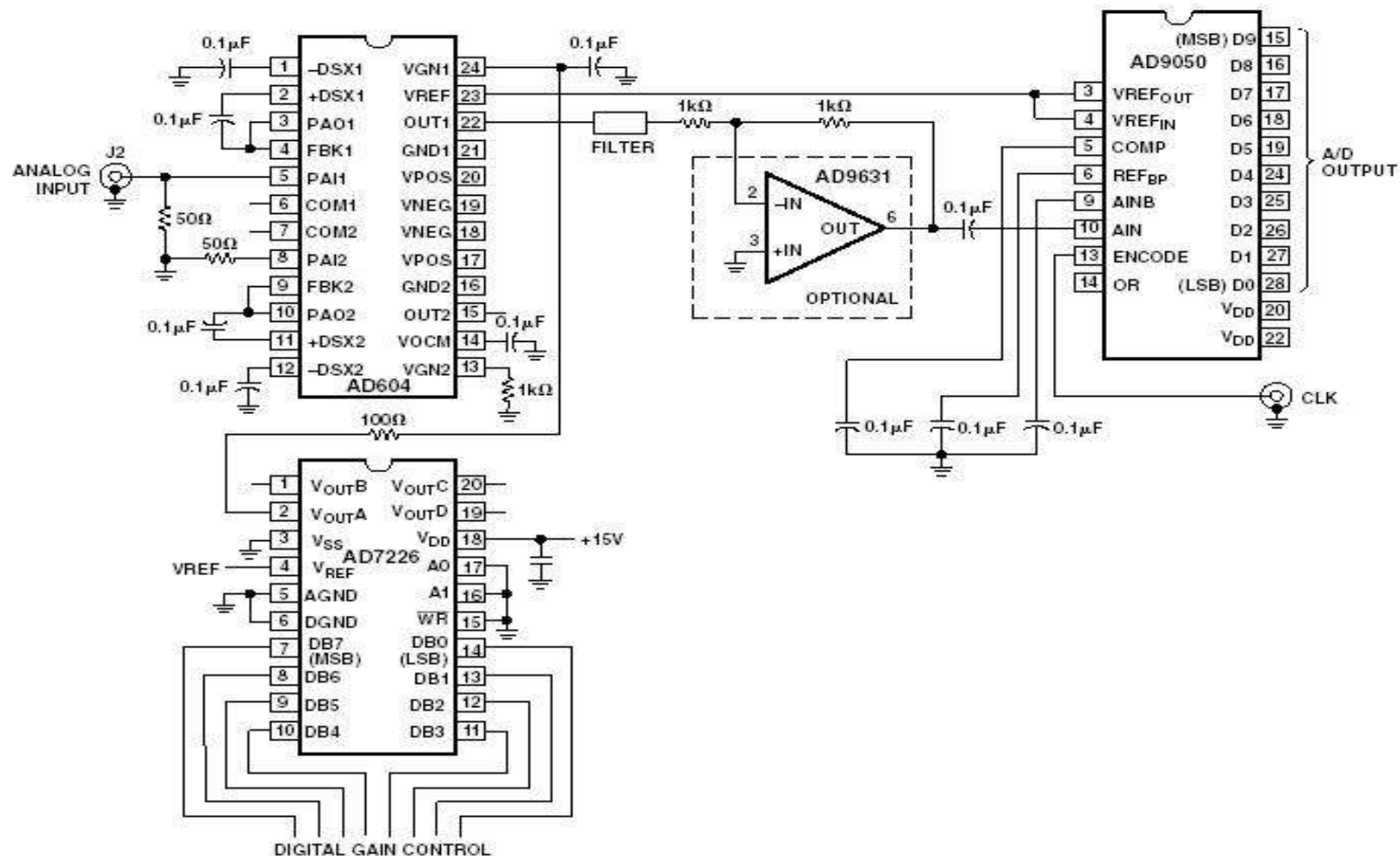


Figure 50. TGC Circuit for Medical Ultrasound Application





# Układy wzmacniające - scalone wzmacniacze mocy klasy AB

## TDA 2052 - SGS Thomson Microelectronics

**TDA 2052** - Hi-Fi audio power amplifier with mute/stand-by

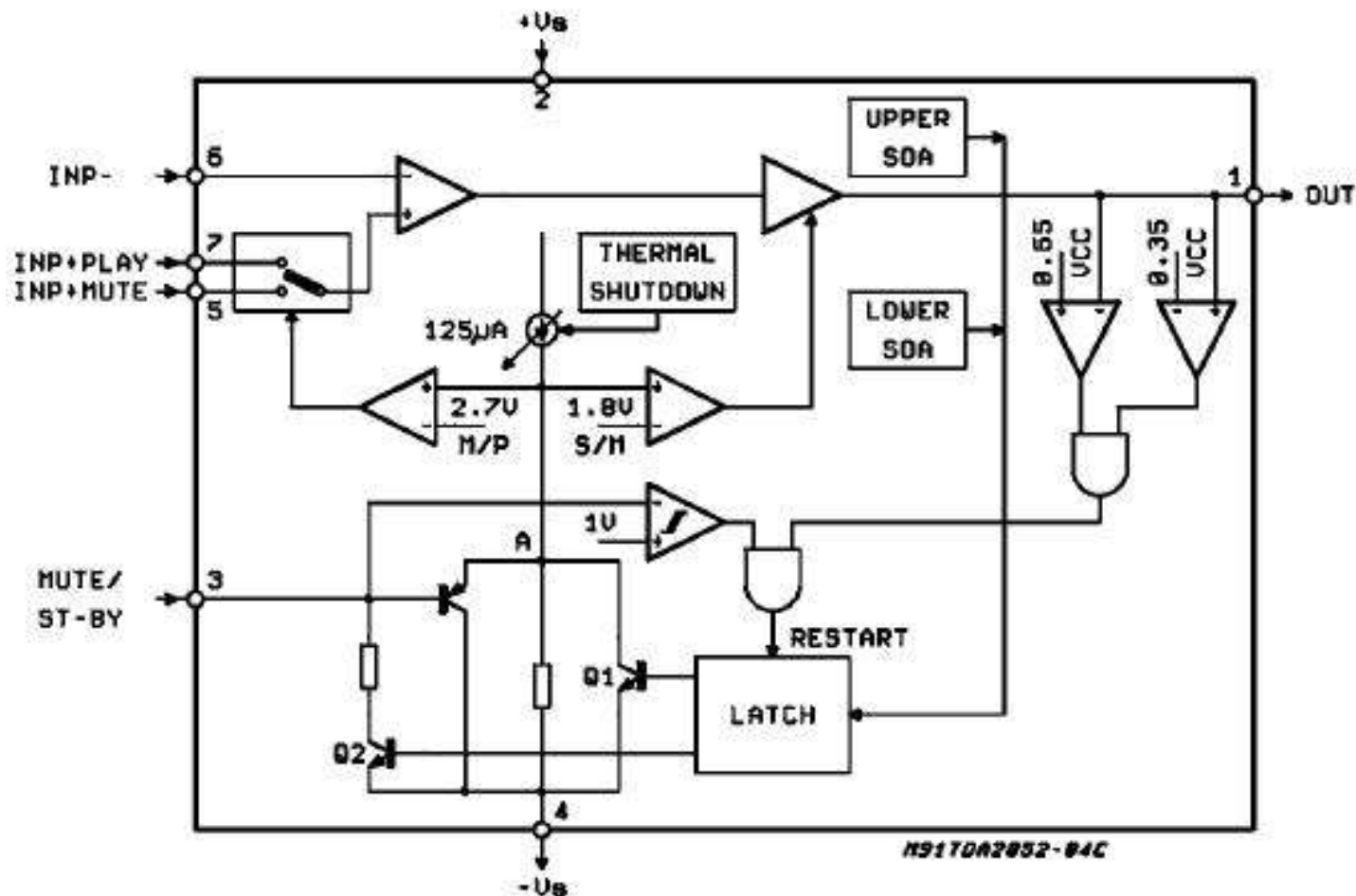
Układ TDA 2052 jest wzmacniaczem mocy klasy Hi-Fi z wbudowanymi funkcjami wyciszenia i uśpienia.

- SUPPLY VOLTAGE RANGE UP TO  $\pm 25V$
- SPLIT SUPPLY OPERATION
- HIGH OUTPUT POWER  
(UP TO 60W MUSIC POWER)
- LOW DISTORTION
- MUTE/STAND-BY FUNCTION
- NO SWITCH ON/OFF NOISE
- AC SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- ESD PROTECTION



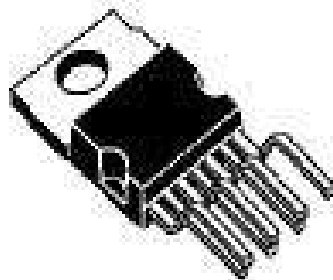
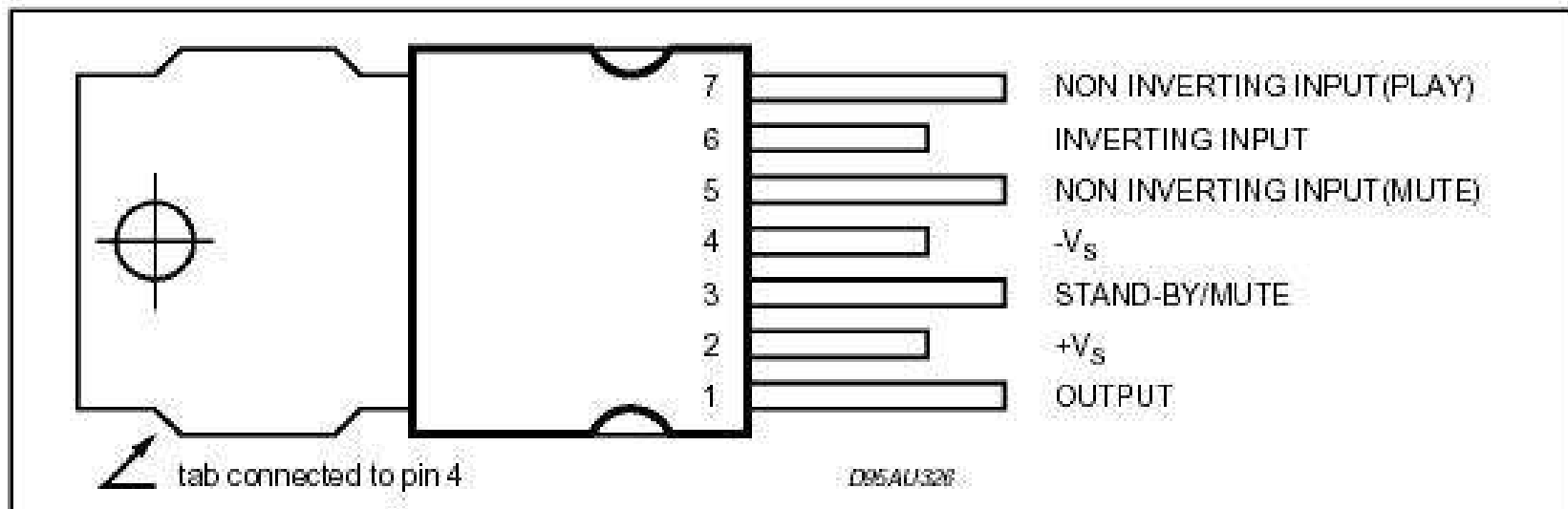
# Układy wzmacniające - scalone wzmacniacze mocy klasy AB

## TDA 2052 - SGS Thomson Microelectronics



# Układy wzmacniające - scalone wzmacniacze mocy klasy AB

## TDA 2052 - SGS Thomson Microelectronics



Heptawatt

ORDERING NUMBER: TDA2052



# Układy wzmacniające - scalone wzmacniacze mocy klasy AB

## TDA 2052 - SGS Thomson Microelectronics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_S$	Supply Range		<u>+6</u>		<u>+25</u>	V
$I_q$	Total Quiescent Current	$V_S = \pm 22V$	20	40	70	mA
$I_b$	Input Bias Current				<u>+0.5</u>	$\mu A$
$V_{OS}$	Input Offset Voltage				<u>+15</u>	mV
$I_{OS}$	Input Offset Current				<u>+200</u>	nA
$P_O$	Musical Output Power IEC268-3 Rules (*)	$V_S = \pm 22.5V, R_L = 4\Omega$ , $d = 10\%, t = 1s$	50	60		W
$P_O$	Output Power (continuous RMS)	$d = 10\%$				
		$R_L = 4\Omega$	35	40		W
		$R_L = 8\Omega$		22		W
		$V_S = \pm 22V, R_L = 8\Omega$	30	33		W
		$d = 1\%$				
		$R_L = 4\Omega$		32		W
		$R_L = 8\Omega$		17		W
		$V_S = \pm 22V, R_L = 8\Omega$		28		W
d	Total Harmonic Distortion	$R_L = 4\Omega$ $P_O = 0.1$ to $20W$ ; $f = 100Hz$ to $15KHz$		0.1	0.7	%
		$V_S \pm 22V, R_L = 8\Omega$ $P_O = 0.1$ to $20W$ ; $f = 100Hz$ to $15KHz$		0.1	0.5	%
SR	Slew Rate		3	5		V/ $\mu s$
$G_V$	Open Loop Voltage Gain			80		dB
$e_N$	Total Input Noise	A Curve $f = 20Hz$ to $20KHz$		2 3	10	$\mu V$ $\mu V$
$R_i$	Input Resistance		500			K $\Omega$
SVR	Supply Voltage Rejection	$f = 100Hz, V_{ripple} = 1V_{RMS}$	40	50		dB
$T_S$	Thermal Shutdown			145		$^{\circ}C$



# Układy wzmacniające - scalone wzmacniacze mocy klasy AB

## TDA 2052 - SGS Thomson Microelectronics

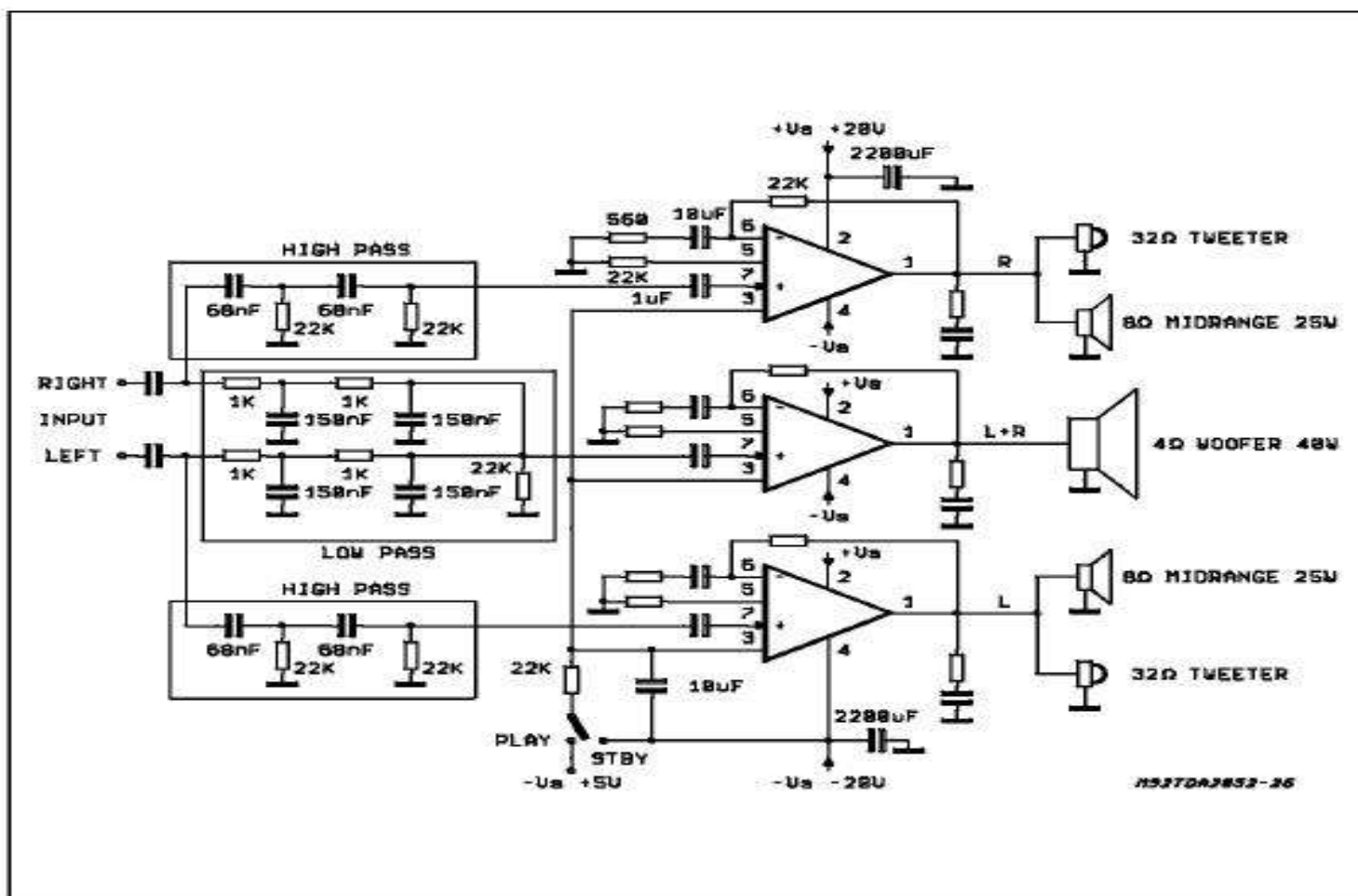
MUTE/STAND-BY FUNCTION (Ref.  $-V_S$ )

$V_{T_{ST-BY}}$	Stand-by - Threshold		1	1.8		V
$V_{T_{PLAY}}$	Play Threshold			2.7	4	V
$I_{q_{ST-BY}}$	Quiescent Current @ Stand-by	$V_{pin 3} = 0.5V$		1	3	mA
$ATT_{ST-BY}$	Stand-by Attenuation		70	90		dB
$I_{pin3}$	Pin 3 Current @ Stand-by			-1	$\pm 10$	$\mu A$

Comp.	Value	Purpose	Larger Than	Smaller Than
R1	22K $\Omega$ (*)	Input Impedance	Increase of Input Impedance	Decrease of Input Impedance
R2	560 $\Omega$	Closed Loop Gain set to 32dB (**)	Decrease of Gain	Increase of Gain
R3	22K $\Omega$ (*)		Increase of Gain	Decrease of Gain
R4	22K $\Omega$ (*)	Input Impedance @ Mute		
R5	22K $\Omega$	Stand-by Time Constant		
R6	4.7 $\Omega$	Frequency Stability	Danger of oscillations	Danger of oscillations
C1	1 $\mu F$	Input DC Decoupling		Higher Low-frequency cut-off
C2	10 $\mu F$	Feedback DC Decoupling		Higher Low-frequency cut-off
C3	10 $\mu F$	Stand-by Time Constant		
C4	0.100 $\mu F$	Frequency Stability		Danger of Oscillations
C5, C6	1000 $\mu F$	Supply Voltage Bypass		

# Układy wzmacniające - scalone wzmacniacze mocy klasy AB TDA 2052 - SGS Thomson Microelectronics

**Figure 18: Multiway Application Circuit**





# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TDA 7480 - SGS Thomson Microelectronics

**TDA 7480** - 10W mono Class-D power amplifier

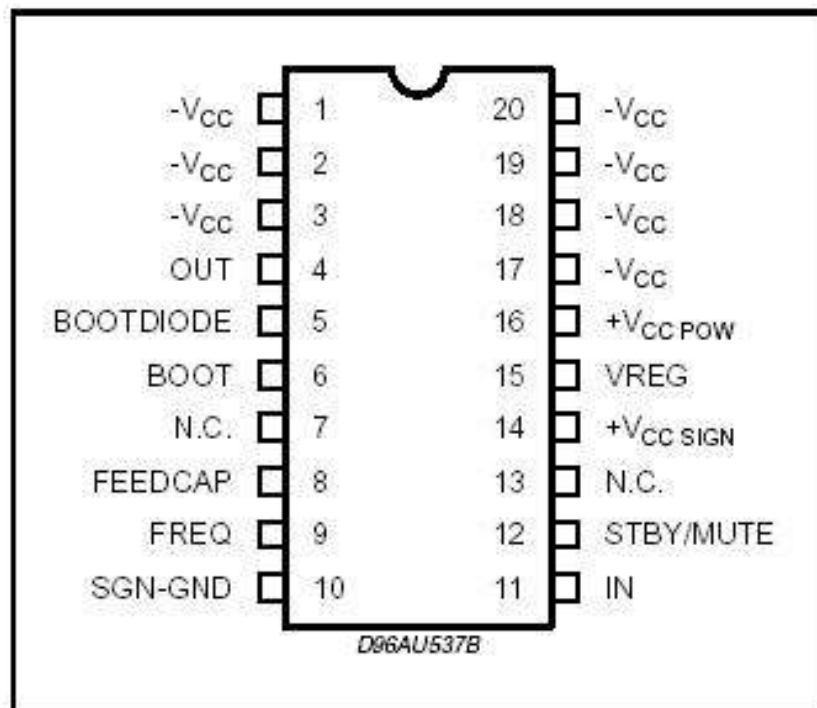
Układ TDA 7480 jest monofonicznym wzmacniaczem mocy klasy D o mocy wyjściowej równej 10W.

- 10W OUTPUT POWER:  
 $R_L = 8\Omega/4\Omega$ ; THD = 10%
- HIGH EFFICIENCY
- NO HEATSINK
- SPLIT SUPPLY
- OVERVOLTAGE PROTECTION
- ST-BY AND MUTE FEATURES
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

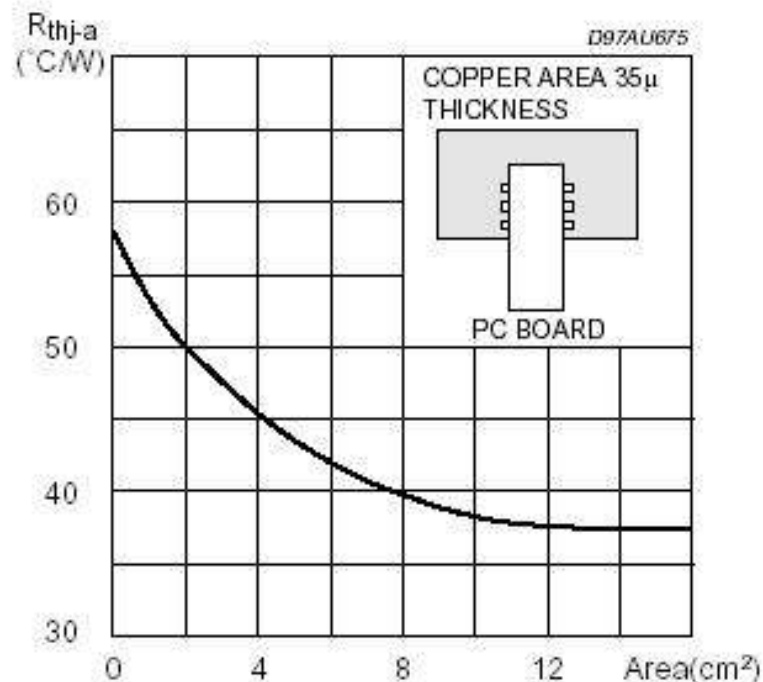
# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TDA 7480 - SGS Thomson Microelectronics

PIN CONNECTION (Top view)



R<sub>thj-a</sub> with "on board" Square Heatsink vs. copper area.







# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TDA 7480 - SGS Thomson Microelectronics

### PIN FUNCTIONS

N.	Name	Function
1	-V <sub>cc</sub>	NEGATIVE SUPPLY.
2	-V <sub>cc</sub>	NEGATIVE SUPPLY.
3	-V <sub>cc</sub>	NEGATIVE SUPPLY.
4	OUT	PWM OUTPUT
5	BOOTDIODE	BOOTSTRAP DIODE ANODE
6	BOOT	BOOTSTRAP CAPACITOR
7	NC	NOT CONNECTED
8	FEEDCAP	FEEDBACK INTEGRATING CAPACITANCE
9	FREQUENCY	SETTING FREQUENCY RESISTOR
10	SGN-GND	SIGNAL GROUND
11	IN	INPUT
12	ST-BY-MUTE	ST-BY/ MUTE CONTROL PIN
13	NC	NOT CONNECTED
14	+V <sub>cc</sub> SIGN	POSITIVE SIGNAL SUPPLY
15	VREG	10V INTERNAL REGULATOR
16	+V <sub>cc</sub> POW	POSITIVE POWER SUPPLY
17	-V <sub>cc</sub>	NEGATIVE SUPPLY (TO BE CONNECTED TO PIN 16 VIA C5)
18	-V <sub>cc</sub>	NEGATIVE SUPPLY
19	-V <sub>cc</sub>	NEGATIVE SUPPLY
20	-V <sub>cc</sub>	NEGATIVE SUPPLY



# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TDA 7480 - SGS Thomson Microelectronics

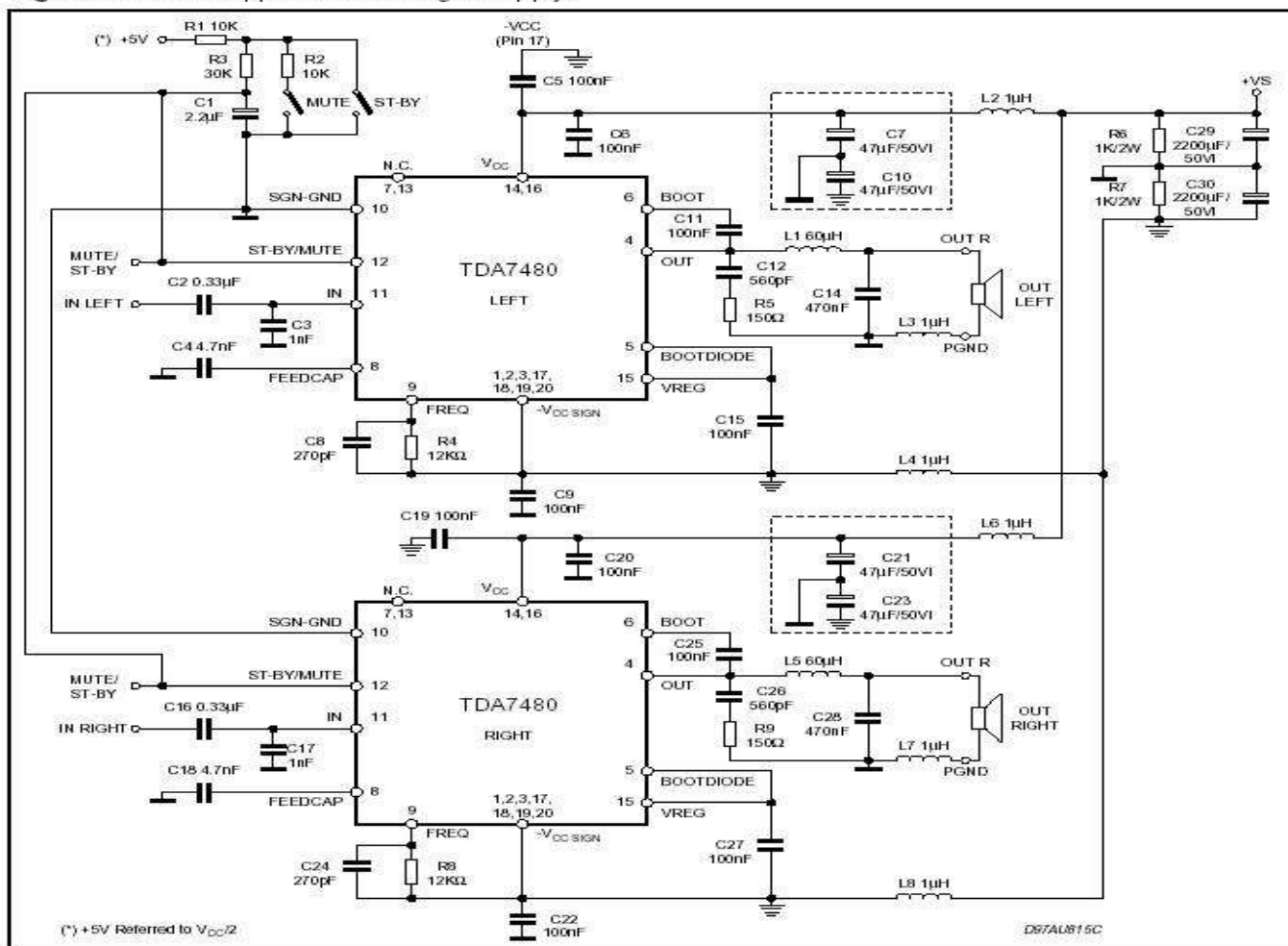
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_S$	Supply Range		$\pm 10$		$\pm 16$	V
$I_q$	Total Quiescent Current	$R_L = \infty$ ; NO LC Filter		25	40	mA
$V_{OS}$	Output Offset Voltage	Play Condition	-50		+50	mV
$P_O$	Output Power	THD = 10% THD = 1%	8.5 6	10 7		W W
		$R_L = 4\Omega$ $V_{CC} = \pm 10.5V$ THD = 10% THD = 1%		10 7		W W
$P_d$ (*)	Dissipated Power at 1W Output Power	$R_f = 12K\Omega$ $P_O = 1W$		1		W
$P_{DMAX}$	Maximum Dissipated Power	$P_O = 10W$ THD 10% $R_{th-j-amb} = 38^\circ C/W$ (Area $12cm^2$ )		1.8		W
$\eta$	Efficiency $\equiv \frac{P_O}{P_O + P_D} \equiv \frac{P_O}{P_i}$ (**)	THD 10% $R_{th-j-amb} = 38^\circ C/W$ (Area $12cm^2$ )	80	85		%
THD	Total Harmonic Distortion	$R_L = 8\Omega$ ; $P_O = 0.5W$		0.1		%
$I_{max}$	Overcurrent Protection Threshold	$R_L = 0$	3.5	5		A
$T_j$	Thermal Shut-down Junction Temperature			150		$^\circ C$
$G_v$	Closed Loop Gain		29	30	31	dB
$e_N$	Total Input Noise	A Curve $f = 20Hz$ to $22KHz$		7 12		$\mu V$ $\mu V$
$R_i$	Input Resistance		20	30		$K\Omega$
SVR	Supply Voltage Rejection	$f = 100Hz$ ; $V_r = 0.5$	46	60		dB
$T_r, T_f$	Rising and Falling Time			50		ns
$R_{DS(on)}$	Power Transistor on Resistance			0.4		$\Omega$
$F_{SW}$	Switching Frequency		100	120	140	KHz
$F_{SW\_OP}$	Switching Frequency Operative Range		100		200	KHz
$B_F$	Zero Signal Frequency Constant (***)			$1.4 \times 10^9$		Hz $\Omega$
$R_F$	Frequency Controller Resistor Range (****)		7	12	14	$K\Omega$



# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TDA 7480 - SGS Thomson Microelectronics

Figure 3: Stereo Application in Single Supply.



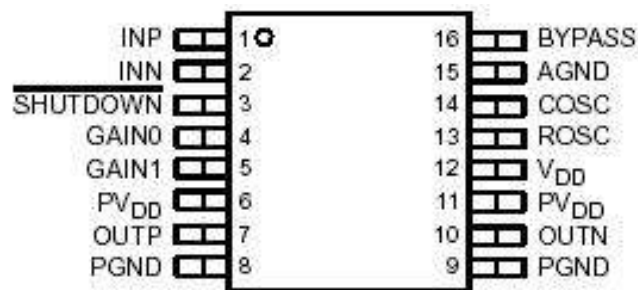
# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TPA 2001 - Texas Instruments

### TPA 2001 - 1W filterless mono Class-D power amplifier

Układ TPA 2001 jest 1W monofonicznym wzmacniaczem mocy klasy D, pracującym bez wyjściowego dolnoprzepustowego filtru LC.

- Modulation Scheme Optimized to Operate Without a Filter
- TSSOP Package Options
- 1 W Into an 8- $\Omega$  Speaker (THD+N<1%)
- <0.2% THD+N at 1 W, 1 kHz, Into an 8- $\Omega$  Load
- Extremely Efficient Third Generation 5-V Class-D Technology:
  - Low-Supply Current (No Filter) . . . 4 mA
  - Low-Supply Current (Filter) . . . 7.5 mA
  - Low-Shutdown Current . . . 0.05  $\mu$ A
  - Low-Noise Floor . . . 40  $\mu$ V<sub>RMS</sub> (No-Weighting Filter)
  - Maximum Efficiency Into 8  $\Omega$ , 75 – 85%
  - 4 Internal Gain Settings . . . 6 – 23.5 dB
  - PSRR . . . –77 dB
- Integrated Depop Circuitry
- Short-Circuit Protection (Short to Battery, Ground, and Load)





# Układy wzmacniające - scalone wzmacniacze mocy klasy D

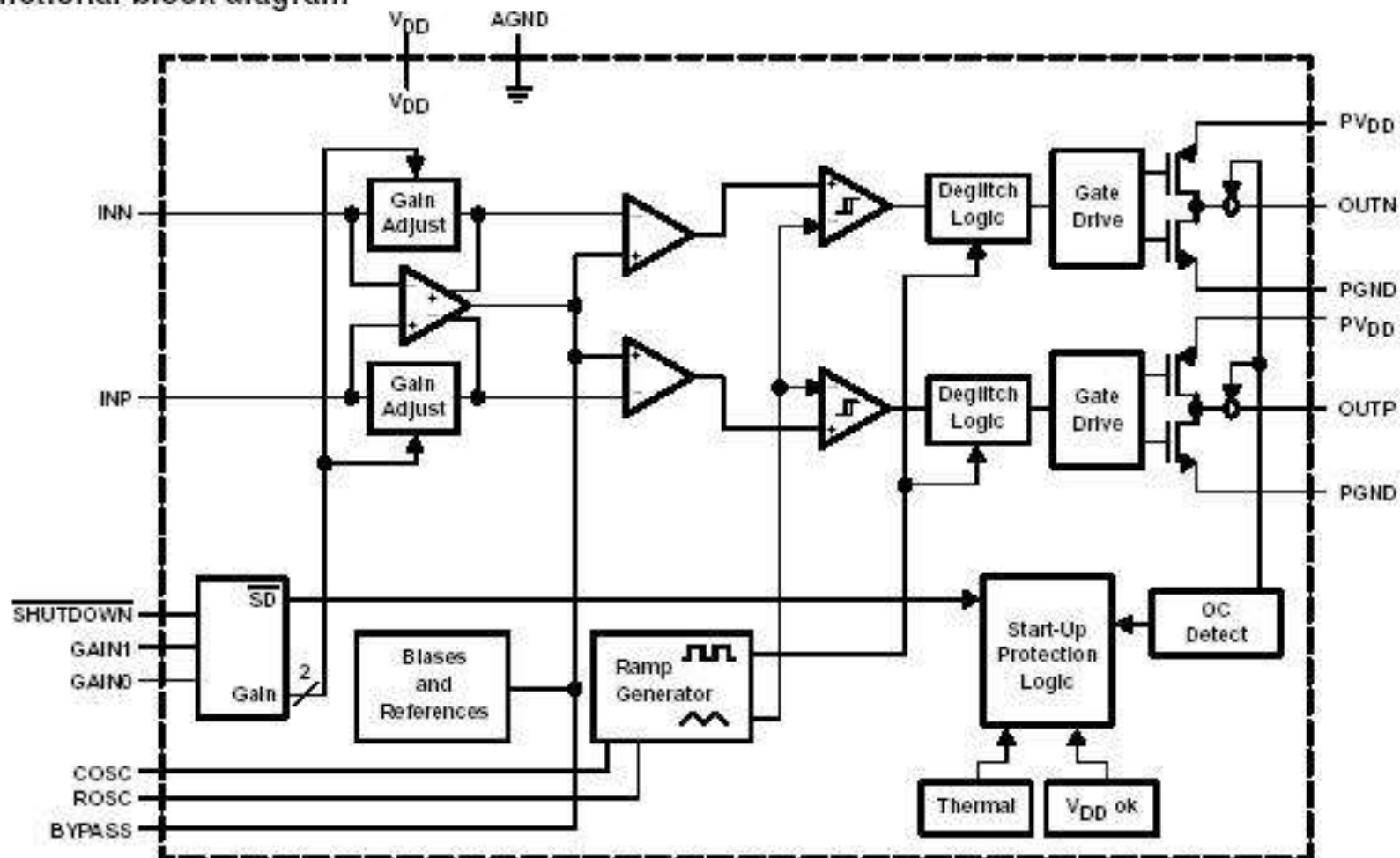
## TPA 2001 - Texas Instruments

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	GQC	PW		
AGND	A3 – A5, B2 – B6 C2 – C6 D2 – D4	15	I	Analog ground
BYPASS	A6	16	I	Connect capacitor to ground for BYPASS voltage filtering.
COSC	B7	14	I	Connect capacitor to ground to set oscillation frequency.
GAIN0	C1	4	I	Bit 0 of gain control (TTL logic level)
GAIN1	D1	5	I	Bit 1 of gain control (TTL logic level)
INN	A1	2	I	Negative differential input
INP	A2	1	I	Positive differential input
OUTN	G7	10	O	Negative BTL output
OUTP	G1	7	O	Positive BTL output
PGND	D5, D6 E2 – E6 F2 – F6 G2 – G6	8, 9	I	High-current grounds
PVDD	E1, E7, F1, F7	6, 11	I	High-current power supplies
ROSC	C7	13	I	Connect resistor to ground to set oscillation frequency.
SHUTDOWN	B1	3	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal, and normal operation if a TTL logic high is placed on this terminal.
VDD	D7	12	I	Analog power supply



# Układy wzmacniające - scalone wzmacniacze mocy klasy D TPA 2001 - Texas Instruments

functional block diagram





# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TPA 2001 - Texas Instruments

electrical characteristics at specified free-air temperature,  $PV_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OS} $ Output offset voltage (measured differentially)	$V_I = 0\text{ V}$ , $A_V = \text{any gain}$			25	mV
PSRR Power supply rejection ratio	$PV_{DD} = 4.9\text{ V to } 5.1\text{ V}$		77		dB
$ I_{IH} $ High-level input current	$PV_{DD} = 5.5\text{ V}$ , $V_I = PV_{DD}$			1	$\mu\text{A}$
$ I_{IL} $ Low-level input current	$PV_{DD} = 5.5\text{ V}$ , $V_I = 0\text{ V}$			1	$\mu\text{A}$
$I_{DD}$ Supply current, no filter (with or without speaker load)			4	6	mA
$I_{DD(SD)}$ Supply current, shutdown mode	GAIN0, GAIN1, SHUTDOWN = 0 V		0.05	20	$\mu\text{A}$

electrical characteristics at specified free-air temperature,  $PV_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OS} $ Output offset voltage (measured differentially)	$V_I = 0\text{ V}$ , $A_V = \text{any gain}$			25	mV
PSRR Power supply rejection ratio	$PV_{DD} = 3.2\text{ V to } 3.4\text{ V}$		61		dB
$ I_{IH} $ High-level input current	$PV_{DD} = 3.3\text{ V}$ , $V_I = PV_{DD}$			1	$\mu\text{A}$
$ I_{IL} $ Low-level input current	$PV_{DD} = 3.3\text{ V}$ , $V_I = 0\text{ V}$			1	$\mu\text{A}$
$I_{DD}$ Supply current, no filter (with or without speaker load)			4	6	mA
$I_{DD(SD)}$ Supply current, shutdown mode			0.05	20	$\mu\text{A}$



# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TPA 2001 - Texas Instruments

operating characteristics,  $PV_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\ \Omega$ , gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power	THD = 1%, $f = 1\text{ kHz}$		1		W
THD + N	Total harmonic distortion plus noise	$P_O = 1\text{ W}$ , $f = 20\text{ Hz to } 20\text{ kHz}$		<0.1%		
$B_{OM}$	Maximum output power bandwidth	THD = 1%		20		kHz
$k_{SVR}$	Supply ripple rejection ratio	$f = 1\text{ kHz}$ , $C_{(BYP)} = 1\ \mu\text{F}$		71		dB
SNR	Signal-to-noise ratio			95		dB
$V_n$	Output noise voltage (no noise weighting filter)	$C_{(BYP)} = 1\ \mu\text{F}$ , $f = <10\text{ Hz to } 22\text{ kHz}$		40		$\mu\text{V(rms)}$
$Z_i$	Input impedance			>15		k $\Omega$

operating characteristics,  $PV_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\ \Omega$ , gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power	THD = 1%, $f = 1\text{ kHz}$		400		mW
THD + N	Total harmonic distortion plus noise	$P_O = 55\text{ mW}$ , $f = 20\text{ Hz to } 20\text{ kHz}$		<0.1%		
$B_{OM}$	Maximum output power bandwidth	THD = 0.7%		20		kHz
$k_{SVR}$	Supply ripple rejection ratio	$f = 1\text{ kHz}$ , $C_{(BYP)} = 1\ \mu\text{F}$		61		dB
SNR	Signal-to-noise ratio			93		dB
$V_n$	Output noise voltage (no noise weighting filter)	$C_{(BYP)} = 1\ \mu\text{F}$ , $f = <10\text{ Hz to } 22\text{ kHz}$		40		$\mu\text{V(rms)}$
$Z_i$	Input impedance			>15		k $\Omega$

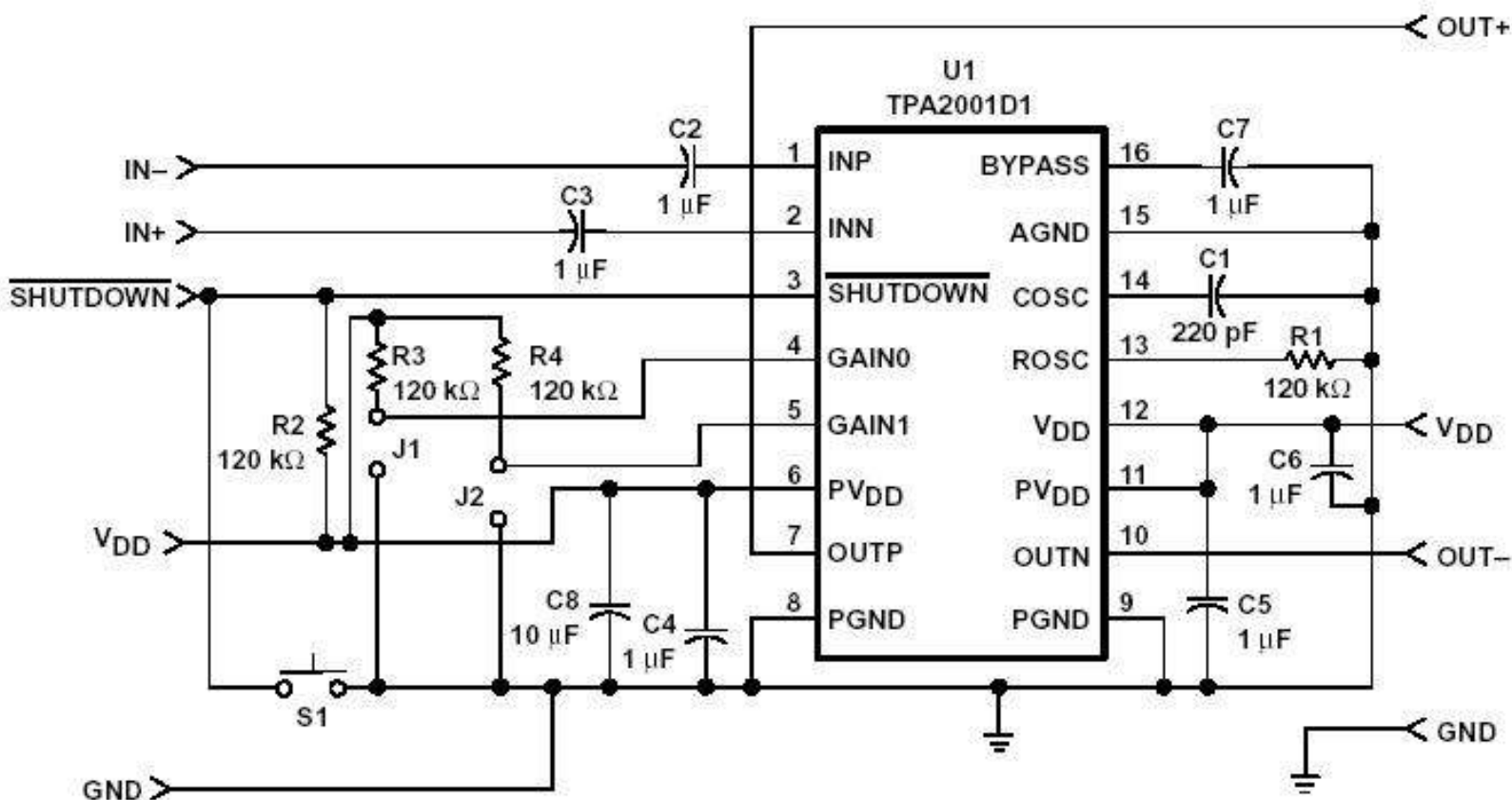




# Układy wzmacniające - scalone wzmacniacze mocy klasy D

## TPA 2001 - Texas Instruments

evaluation circuit





# Demodulatory

## AD 606 - Analog Devices

**AD 606** - 80 dB Demodulating logarithmic amplifier with limiter output

Układ AD 606 jest wzmacniaczem logarytmującym z demodulatorem amplitudy posiadającym także wyjście połączone z wewnętrznym ogranicznikiem amplitudy. Funkcja układu:

$$V_{LOG} = V_Y \log_{10} (V_{IN}/V_X)$$

gdzie:

$V_Y$  - napięcie odpowiadające za nachylenie ch-ki przejściowej układu [V/dB]

$V_X$  - napięcie odniesienia

# Demodulatory

## AD 606 - Analog Devices

### FEATURES

#### Logarithmic Amplifier Performance

-75 dBm to +5 dBm Dynamic Range

$\leq 1.5 \text{ nV}/\sqrt{\text{Hz}}$  Input Noise

Usable to >50 MHz

37.5 mV/dB Voltage Output

On-Chip Low-Pass Output Filter

#### Limiter Performance

$\pm 1 \text{ dB}$  Output Flatness over 80 dB Range

$\pm 3^\circ$  Phase Stability at 10.7 MHz over 80 dB Range

Adjustable Output Amplitude

#### Low Power

+5 V Single Supply Operation

65 mW Typical Power Consumption

CMOS-Compatible Power-Down to 325  $\mu\text{W}$  typ

<5  $\mu\text{s}$  Enable/Disable Time

### APPLICATIONS

Ultrasound and Sonar Processing

Phase-Stable Limiting Amplifier to 100 MHz

Received Signal Strength Indicator (RSSI)

Wide Range Signal and Power Measurement

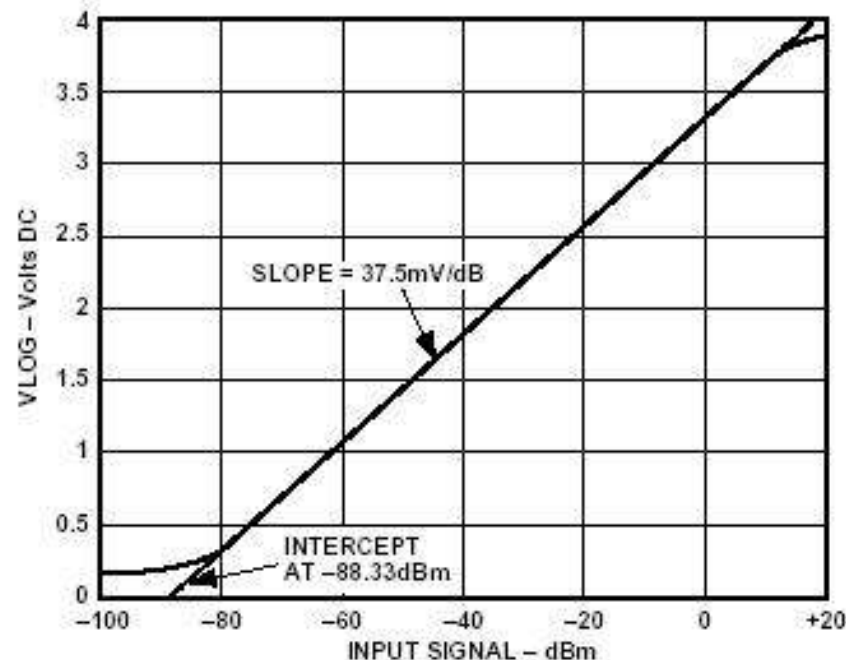


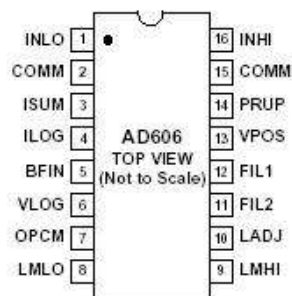
Figure 1. Nominal Transfer Function



# Demodulatory

## AD 606 - Analog Devices

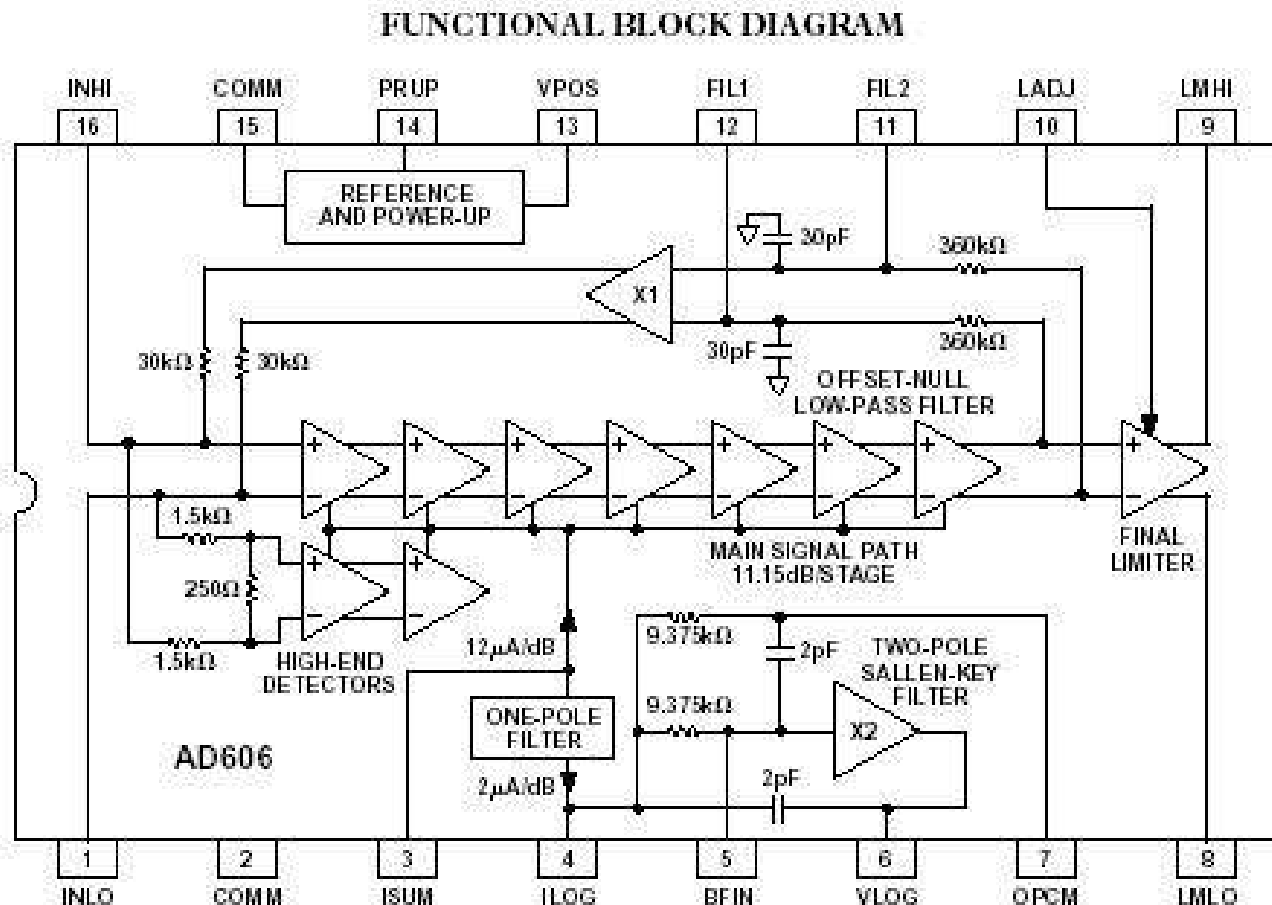
**PIN DESCRIPTION**  
Plastic DIP (N)  
and  
Small Outline (R)  
Packages



Pin	Mnemonic	Function
1	INLO	DIFFERENTIAL RF INPUT -75 dBm to +5 dBm, Inverting, AC Coupled.
2	COMM	POWER SUPPLY COMMON Connect to Ground.
3	ISUM	LOG DETECTOR SUMMING NODE
4	ILOG	LOG CURRENT OUTPUT Normally No Connection; 2 $\mu$ A/dB Output Current.
5	BFIN	BUFFER INPUT Optionally Used to Realize Low Frequency Post-Demodulation Filters.
6	VLOG	BUFFERED LOG OUTPUT 37.5 mV/dB (100 mV to 4.5 V).
7	OPCM	OUTPUT COMMON Connect to Ground.
8	LMLO	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with $R \leq 400 \Omega$ .
9	LMHI	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with $R \leq 400 \Omega$ .
10	LADJ	LIMITER LEVEL ADJUSTMENT Optionally Used to Adjust Limiter Output Current.
11	FIL1	OFFSET LOOP LOW-PASS FILTER Normally No Connection; a Capacitor Between FIL1 and FIL2 May Be Added to Lower the Filter Cutoff Frequency.
12	FIL2	OFFSET LOOP LOW-PASS FILTER Normally No Connection; See Above.
13	VPOS	POSITIVE SUPPLY Connect to +5 V at 13 mA.
14	PRUP	POWER UP CMOS (5 V) Logical High = Device On ( $\approx 65$ mW). CMOS (0 V) Logical Low = Device Off ( $\approx 325 \mu$ W).
15	COMM	POWER SUPPLY COMMON Connect to Ground.
16	INHI	DIFFERENTIAL RF INPUT -75 dBm to +5 dBm, Noninverting, AC-Coupled.

# Demodulatory

## AD 606 - Analog Devices





# Demodulatory

## AD 606 - Analog Devices

Model Parameter	Conditions	Min	AD606J Typ	Max	Units
<b>SIGNAL INPUT</b>					
Log Amp $f_{MAX}$	AC Coupled; Sinusoidal Input		50		MHz
Limiter $f_{MAX}$	AC Coupled; Sinusoidal Input		100		MHz
Dynamic Range			80		dB
Input Resistance	Differential Input	500	2,500		$\Omega$
Input Capacitance	Differential Input		2		pF
<b>SIGNAL OUTPUT</b>					
Limiter Flatness	-75 dBm to +5 dBm Input Signal at 10.7 MHz With Pin 9 to $V_{POS}$ via a 200 $\Omega$ Resistor and Pin 8 to $V_{POS}$ via a 200 $\Omega$ Resistor	-1.5		+1.5	dB
Output Current	At Pins 8 or 9, Proportional to $V_{POS}$ , LADJ Grounded LADJ Open Circuited		1.2 0.48		mA mA
Phase Variation with Input Level	-75 dBm to +5 dBm Input Signal at 10.7 MHz		$\pm 3$		Degrees
<b>LOG (RSSI) OUTPUT</b>					
Nominal Slope	At 10.7 MHz; $(0.0075 \times V_{POS})/\text{dB}$ At 45 MHz		37.5 35		mV/dB mV/dB
Slope Accuracy	Untrimmed at 10.7 MHz	-15	$\pm 5$	+15	%
Intercept	Sinusoidal Input; Independent of $V_{POS}$		-88.33		dBm
Logarithmic Conformance	-75 dBm to +5 dBm Input Signal at 10.7 MHz	-1.5	0.4	+1.5	dB
Nominal Output	Input Level = -75 dBm		0.5		V
	Input Level = -35 dBm		2		V
	Input Level = +5 dBm		3.5		V
Accuracy over Temperature	After Calibration at -35 dBm at 10.7 MHz $T_{MIN}$ to $T_{MAX}$	-3		+3	dB
Video Response Time	From Onset of Input Signal Until Output Reaches 95% of Final Value		400		ns



# Demodulatory

## AD 606 - Analog Devices

POWER-DOWN INTERFACE			
Power-Up Response Time	Time Delay Following HI Transition Until Device Meets Full Specifications	3.5	$\mu\text{s}$
Input Bias Current	AC Coupled with 100 pF Coupling Capacitors	1	nA
	Logical HI Input (See Figure 12)	4	$\mu\text{A}$
POWER SUPPLY			
Operating Range	Zero Signal Input	4.5	5.5
Powered-Up Current	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	13	mA
	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	13	20
Powered-Down Current	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	65	200
	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	65	200

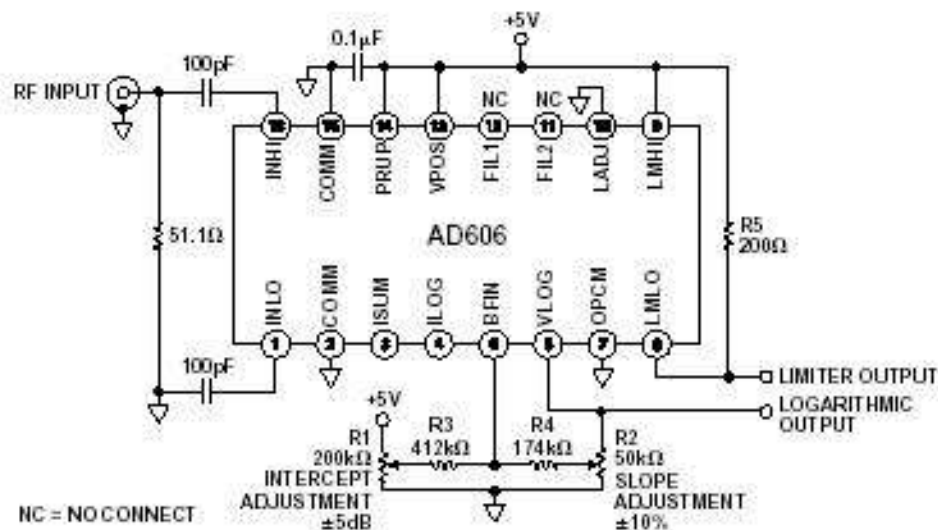


Figure 6. Basic Application Circuit Showing Optional Slope and Intercept Adjustments



# Demodulatory AD 606 - Analog Devices

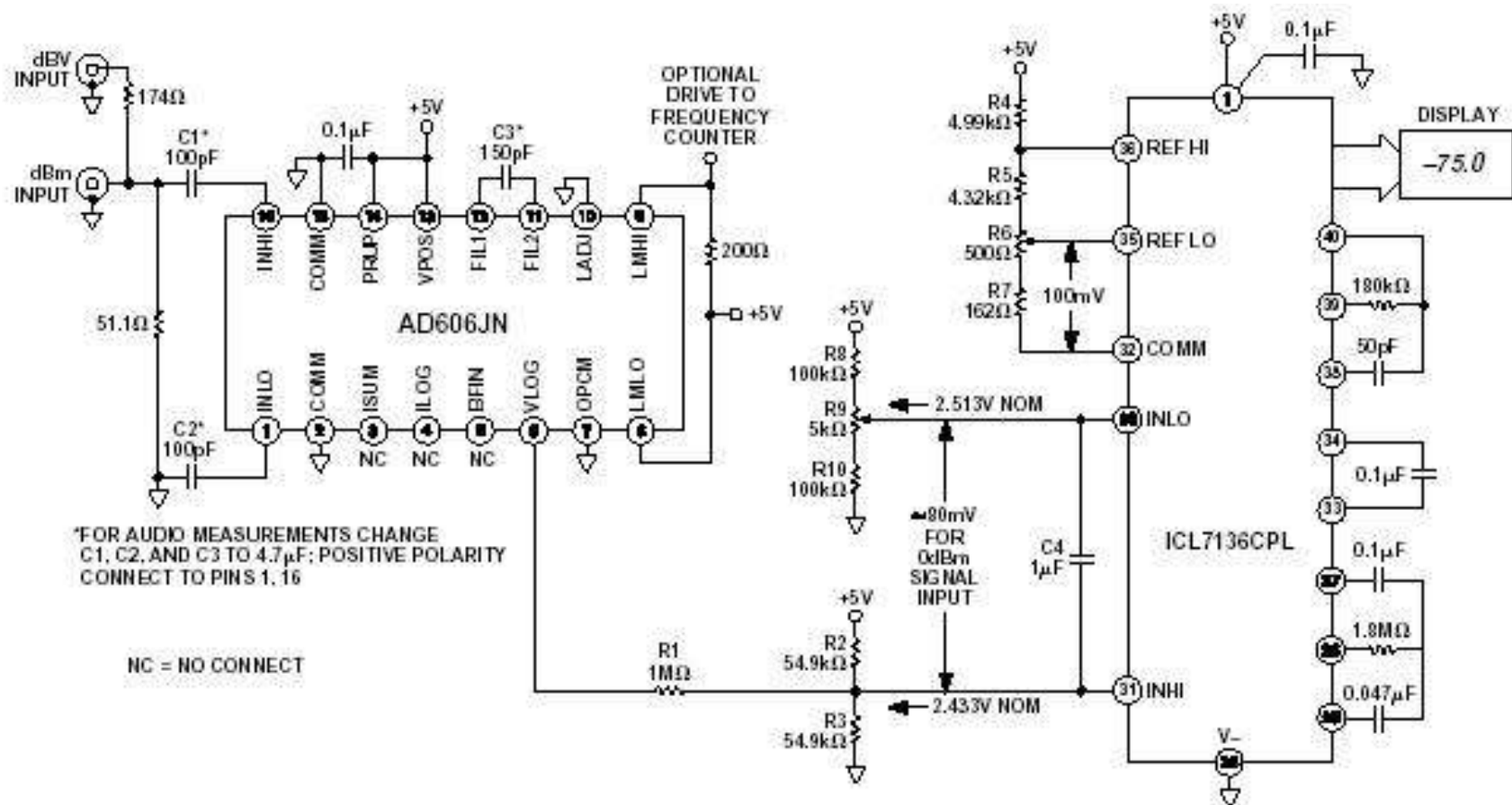


Figure 7. A Low Cost RF Power Meter



# Demodulatory

## AD 606 - Analog Devices

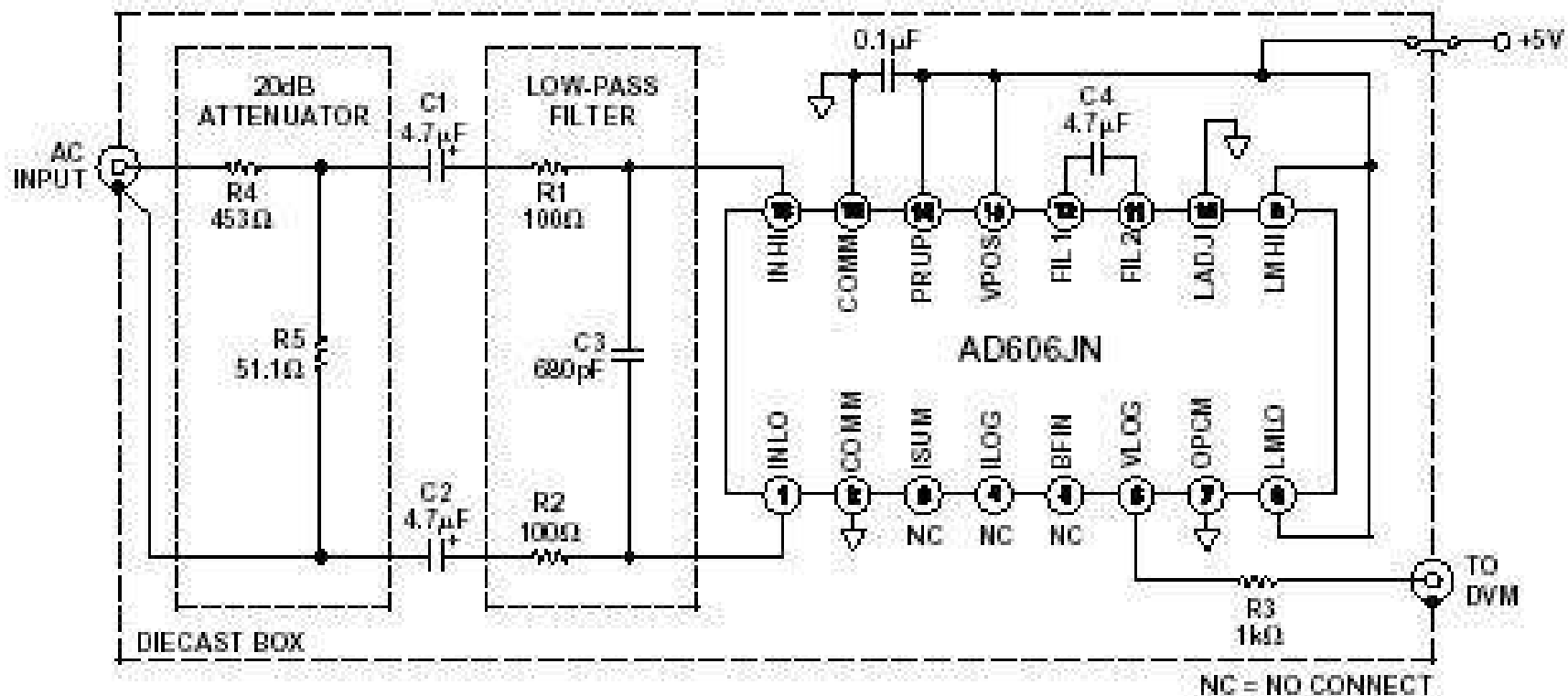


Figure 8. Circuit for Low Frequency Measurements

# Przetworniki RMS - DC

## LTC 1968 - Linear Technology

### LTC 1968 - Precision wide bandwidth RMS-to-DC converter

Układ LTC 1968 jest precyzyjnym, szerokopasmowym przetwornikiem wartości skutecznej napięcia na odpowiadającą jej wartość napięcia stałego

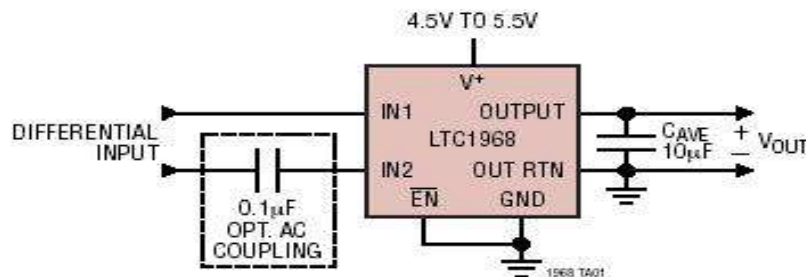
#### APPLICATIONS

- True RMS Digital Multimeters and Panel Meters
- True RMS AC + DC Measurements

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#### TYPICAL APPLICATION

##### Single Supply RMS-to-DC Converter



# Przetworniki RMS - DC

## LTC 1968 - Linear Technology

### FEATURES

- **High Linearity:**  
0.02% Linearity Allows Simple System Calibration
- **Wide Input Bandwidth:**  
Bandwidth to 1% Additional Gain Error: 500kHz  
Bandwidth to 0.1% Additional Gain Error: 150kHz  
3dB Bandwidth Independent of Input Voltage Amplitude
- **No-Hassle Simplicity:**  
True RMS-DC Conversion with Only One External Capacitor  
Delta Sigma Conversion Technology
- **Ultralow Shutdown Current:**  
0.1 $\mu$ A
- **Flexible Inputs:**  
Differential or Single Ended  
Rail-to-Rail Common Mode Voltage Range  
Up to 1V<sub>PEAK</sub> Differential Voltage
- **Flexible Output:**  
Rail-to-Rail Output  
Separate Output Reference Pin Allows Level Shifting
- **Small Size:**  
Space Saving 8-Pin MSOP Package

# Przetworniki RMS - DC

## LTC 1968 - Linear Technology

### PIN FUNCTIONS

**GND (Pin 1):** Ground. The power return pin.

**IN1 (Pin 2):** Differential Input. DC coupled (polarity is irrelevant).

**IN2 (Pin 3):** Differential Input. DC coupled (polarity is irrelevant).

**V<sub>OUT</sub> (Pin 5):** Output Voltage. Pin 5 is high impedance. The RMS averaging is accomplished with a single shunt capacitor from Pin 5 to OUT RTN. The transfer function is given by:

$$(V_{OUT} - OUT\ RTN) = \sqrt{\text{Average}[(IN2 - IN1)^2]}$$

**OUT RTN (Pin 6):** Output Return. The output voltage is created relative to this pin. The V<sub>OUT</sub> and OUT RTN pins are not balanced and this pin should be tied to a low impedance, both AC and DC. Although Pin 6 is often tied to GND, it can also be tied to any arbitrary voltage:

$$GND < OUT\ RTN < (V^+ - \text{Max Output})$$

**V<sup>+</sup> (Pin 7):** Positive Voltage Supply. 4.5V to 5.5V.

**ENABLE (Pin 8):** An Active-Low Enable Input. LTC1968 is debiased if open circuited or driven to V<sup>+</sup>. For normal operation, pull to GND.



$$T_{JMAX} = 150^{\circ}\text{C}, \theta_{JA} = 220^{\circ}\text{C/W}$$



# Przetworniki RMS - DC

## LTC 1968 - Linear Technology

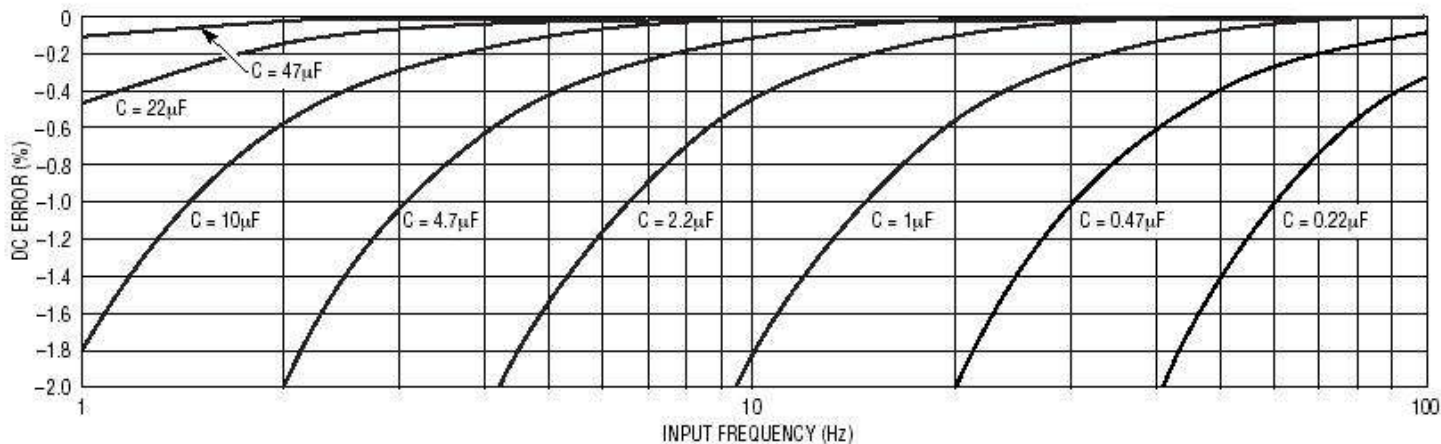


Figure 6. DC Error vs Input Frequency

1988 F08

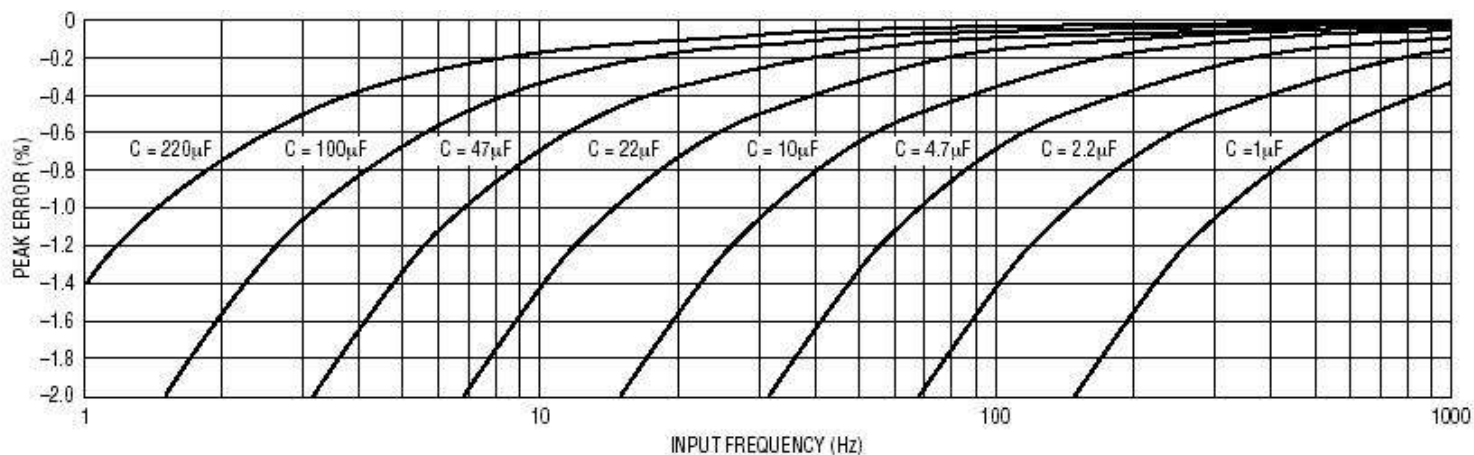


Figure 8. Peak Error vs Input Frequency with One Cap Averaging

1988 F08

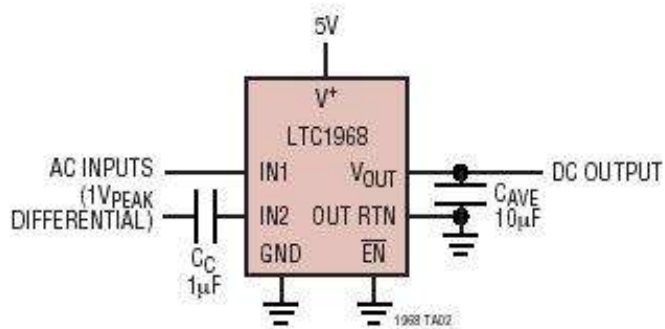


# Przetworniki RMS - DC

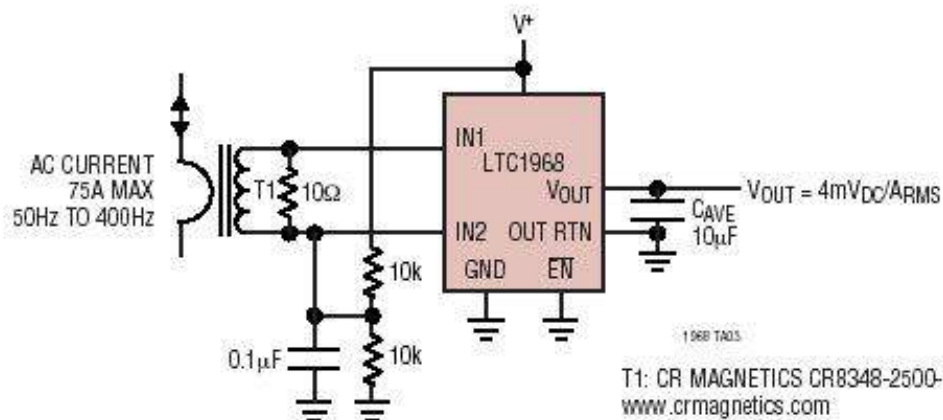
## LTC 1968 - Linear Technology

### TYPICAL APPLICATIONS

5V Single Supply, Differential,  
AC-Coupled RMS-to-DC Converter



Single Supply RMS Current Measurement

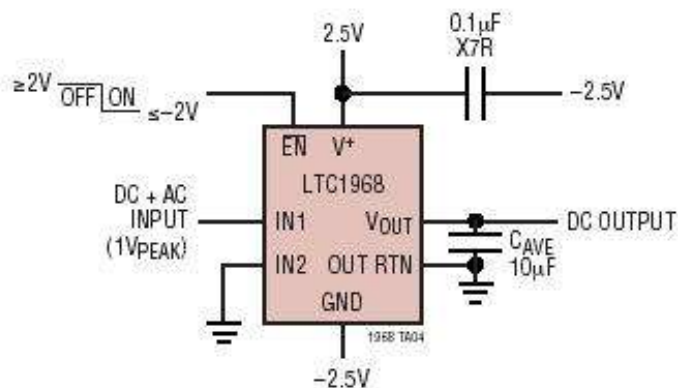


# Przetworniki RMS - DC

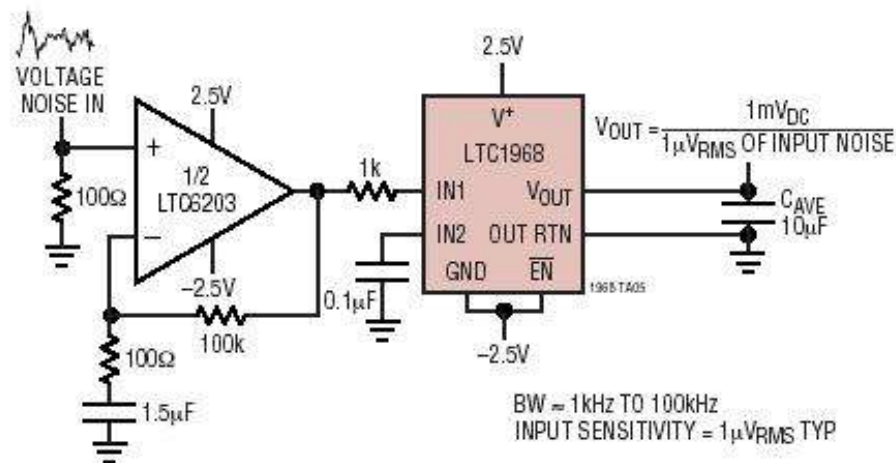
## LTC 1968 - Linear Technology

### TYPICAL APPLICATIONS

$\pm 2.5V$  Supplies, Single Ended, DC-Coupled  
RMS-to-DC Converter with Shutdown



### RMS Noise Measurement







# Filtry C - przełączane

## LTC 1068 - Linear Technology

**LTC 1068** - Clock-tunable, Quad second order, filter building block

Układ LTC 1068 jest uniwersalnym, poczwórnym, C-przełączanym filtrem drugiego rzędu, strojonym częstotliwością zegara zewnętrznego.

### FEATURES

- Four Identical 2nd Order Filter Sections in an SSOP Package
- 2nd Order Section Center Frequency Error:  $\pm 0.3\%$  Typical and  $\pm 0.8\%$  Maximum
- Low Noise per 2nd Order Section,  $Q \leq 5$ :  
LTC1068-200  $50\mu V_{RMS}$ , LTC1068  $50\mu V_{RMS}$   
LTC1068-50  $75\mu V_{RMS}$ , LTC1068-25  $90\mu V_{RMS}$
- Low Power Supply Current: 4.5mA, Single 5V, LTC1068-50
- Operation with  $\pm 5V$  Power Supply, Single 5V Supply or Single 3.3V Supply

### APPLICATIONS

- Lowpass or Highpass Filters:  
LTC1068-200, 0.5Hz to 25kHz; LTC1068, 1Hz to 50kHz; LTC1068-50, 2Hz to 50kHz; LTC1068-25, 4Hz to 200kHz
- Bandpass or Bandreject (Notch) Filters:  
LTC1068-200, 0.5Hz to 15kHz; LTC1068, 1Hz to 30kHz; LTC1068-50, 2Hz to 30kHz; LTC1068-25, 4Hz to 140kHz

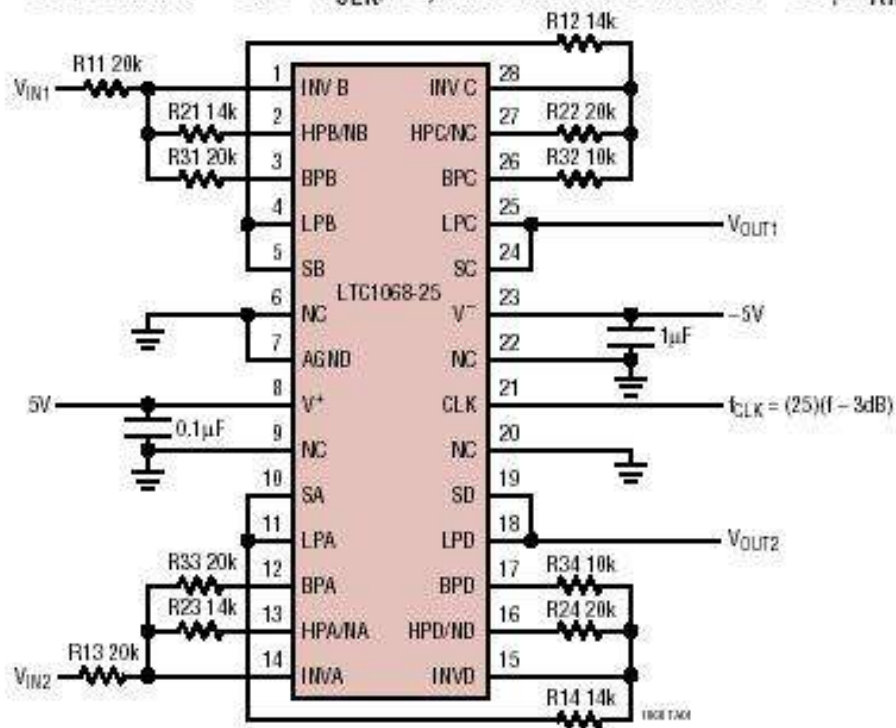


# Filtry C - przełączane

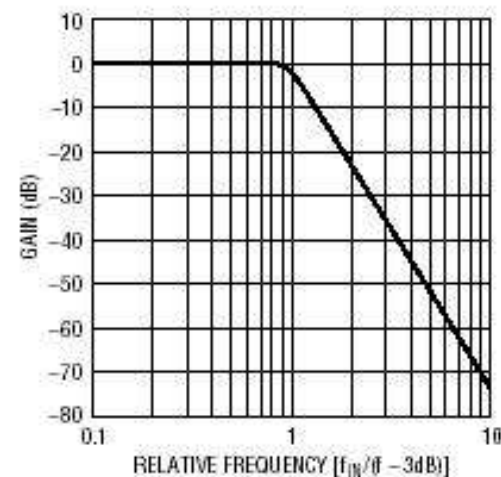
## LTC 1068 - Linear Technology

### TYPICAL APPLICATION

Dual, Matched, 4th Order Butterworth Lowpass Filters, Clock-Tunable Up to 200kHz  $f - 3\text{dB} = f_{\text{CLK}}/25$ , 4th Order Filter Noise =  $60\mu\text{V}_{\text{RMS}}$



Gain vs Frequency





# Filtry C - przełączane

## LTC 1068 - Linear Technology

### PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>6 PACKAGE 28-LEAD PLASTIC SSOP <math>T_{JMAX} = 110^{\circ}\text{C}</math>, <math>\theta_{JA} = 95^{\circ}\text{C/W}</math></p>	<p>TOP VIEW</p> <p>8 PACKAGE 24-LEAD PDIP <math>T_{JMAX} = 110^{\circ}\text{C}</math>, <math>\theta_{JA} = 65^{\circ}\text{C/W}</math></p>
ORDER PART NUMBER	ORDER PART NUMBER
<p>LTC1068CG      LTC1068IG LTC1068-200CG    LTC1068-200IG LTC1068-50CG    LTC1068-50IG LTC1068-25CG    LTC1068-25IG</p>	<p>LTC1068CN LTC1068IN</p>
<p><b>Order Options</b> Tape and Reel: Add #TR Lead Free: Add #PBF    Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a></p>	



# Filtry C - przełączane

## LTC 1068 - Linear Technology

### ELECTRICAL CHARACTERISTICS

LTC1068 (Internal Op Amps). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			3.14		$\pm 5.5$	V
Voltage Swings	$V_S = 3.14V$ , $R_L = 5k$ (Note 2)	●	1.2	1.6		V <sub>p-p</sub>
	$V_S = 4.75V$ , $R_L = 5k$ (Note 3)	●	2.6	3.2		V <sub>p-p</sub>
	$V_S = \pm 5V$ , $R_L = 5k$	●	$\pm 3.4$	$\pm 4.1$		V
Output Short-Circuit Current (Source/Sink)	$V_S = \pm 4.75V$			17/6		mA
	$V_S = \pm 5V$			20/15		mA
DC Open-Loop Gain	$R_L = 5k$			85		dB
GBW Product	$V_S = \pm 5V$			6		MHz
Slew Rate	$V_S = \pm 5V$			10		V/ $\mu s$
Analog Ground Voltage (Note 4)	$V_S = 5V$ , Voltage at AGND			$2.5V \pm 2\%$		V



# Filtry C - przełączane

## LTC 1068 - Linear Technology

### ELECTRICAL CHARACTERISTICS

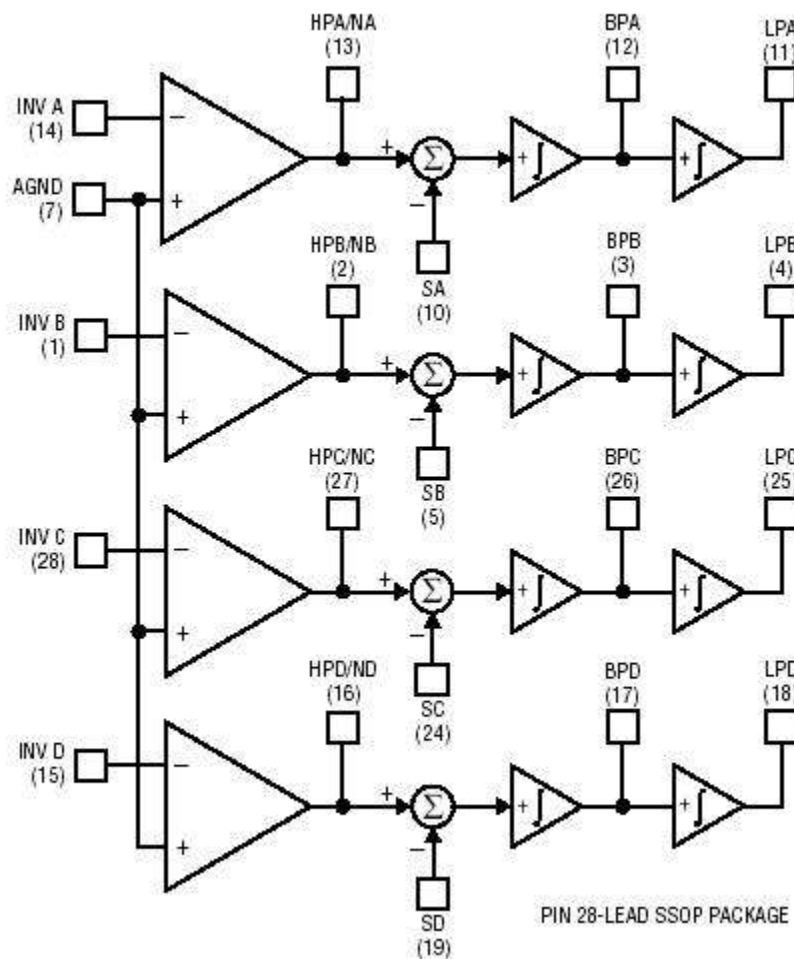
LTC1068 (Complete Filter). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock-to-Center Frequency Ratio (Note 5)	$V_S = 4.75V$ , $f_{CLK} = 1MHz$ , Mode 1 (Note 3), $f_0 = 10kHz$ , $Q = 5$ , $V_{IN} = 0.5V_{RMS}$ , $R1 = R3 = 49.9k$ , $R2 = 10k$	●	100 ± 0.3	100 ± 0.8 100 ± 0.9	% %
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , Mode 1, $f_0 = 10kHz$ , $Q = 5$ , $V_{IN} = 1V_{RMS}$ , $R1 = R3 = 49.9k$ , $R2 = 10k$	●	100 ± 0.3	100 ± 0.8 100 ± 0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	$V_S = 4.75V$ , $f_{CLK} = 1MHz$ , $Q = 5$ (Note 3)	●	± 0.25	± 0.9	%
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , $Q = 5$	●	± 0.25	± 0.9	%
Q Accuracy (Note 5)	$V_S = 4.75V$ , $f_{CLK} = 1MHz$ , $Q = 5$ (Note 3)	●	± 1	± 3	%
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , $Q = 5$	●	± 1	± 3	%
$f_0$ Temperature Coefficient			± 1		ppm/°C
Q Temperature Coefficient			± 5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , $V_{OS1}$ (DC Offset of Input Inverter)	●	0	± 15	mV
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , $V_{OS2}$ (DC Offset of First Integrator)	●	± 2	± 25	mV
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$ , $V_{OS3}$ (DC Offset of Second Integrator)	●	± 5	± 40	mV
Clock Feedthrough	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$		0.1		mV <sub>RMS</sub>
Max Clock Frequency (Note 6)	$V_S = \pm 5V$ , $Q \leq 2.0$ , Mode 1		5.6		MHz
Power Supply Current	$V_S = 3.14V$ , $f_{CLK} = 1MHz$ (Note 2)	●	3.5	8	mA
	$V_S = 4.75V$ , $f_{CLK} = 1MHz$ (Note 3)	●	6.5	11	mA
	$V_S = \pm 5V$ , $f_{CLK} = 1MHz$	●	9.5	15	mA

# Filtry C - przełączane

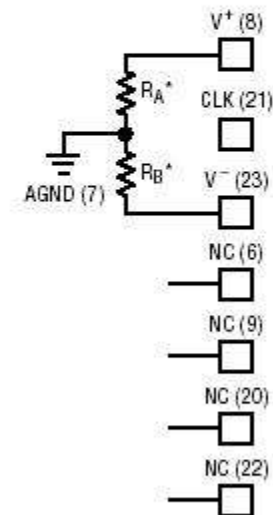
## LTC 1068 - Linear Technology

### BLOCK DIAGRAM



DEVICE	$R_A$	$R_B$
LTC1068		
LTC1068-200	10k	10k
LTC1068-25		
LTC1068-50	11.3k	8.6k

\*THE RATIO  $R_A/R_B$  VARIES  $\pm 2\%$





# Filtry C - przełączane

## LTC 1068 - Linear Technology

### Projektowania -FCAD

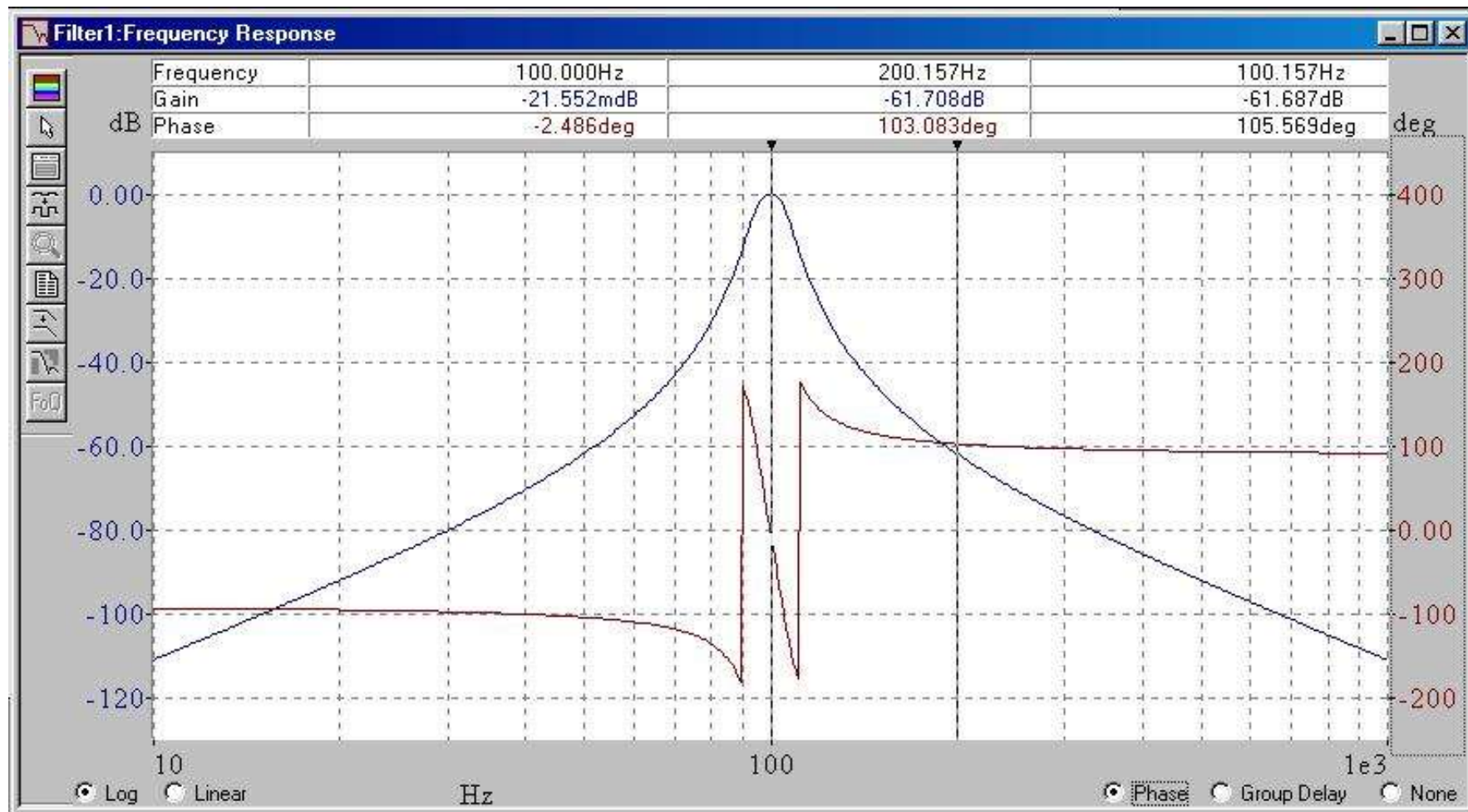
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# Filtry C - przełączane

## LTC 1068 - Linear Technology

### Projektowania -FCAD





# Filtry C - przełączane

## LTC 1068 - Linear Technology

### Projektowania -FCAD

FilterCAD - [Filter1:Enhanced Implement]

File Edit View Implement Window Help

Untitled

Filter Response: Bessel  
Filter Type: Bandpass  
Order: 6

Passband Ripple: 0.000dB  
Stopband Attenuation: 40.000dB  
Center Frequency: 100.000Hz  
Passband Width: 10.000Hz  
Stopband Width: 120.000Hz

☒ Switched Capacitor ☐ Active RC

IC Ratio Supply Clock IC Supply

1068-200200:1 5 20000 Hz

Package: SSOP28 Temp. Range: 0 to 70 ☒ Standard Resistor Values ☒ Low Power

Mode Selection

Swap Fo/Q Swap Fn/Qn Swap All

Fo	Q	Fn	Qn	type	mode	Rnrm
99.8749	7.5264	-	-	BP	1b	10
94.9796	9.5115	-	-	BP	1b	10
105.0225	9.5115	-	-	BP	2	10
-	-	-	-	-	-	-
-	-	-	-	-	-	-
-	-	-	-	-	-	-
-	-	-	-	-	-	-
-	-	-	-	-	-	-

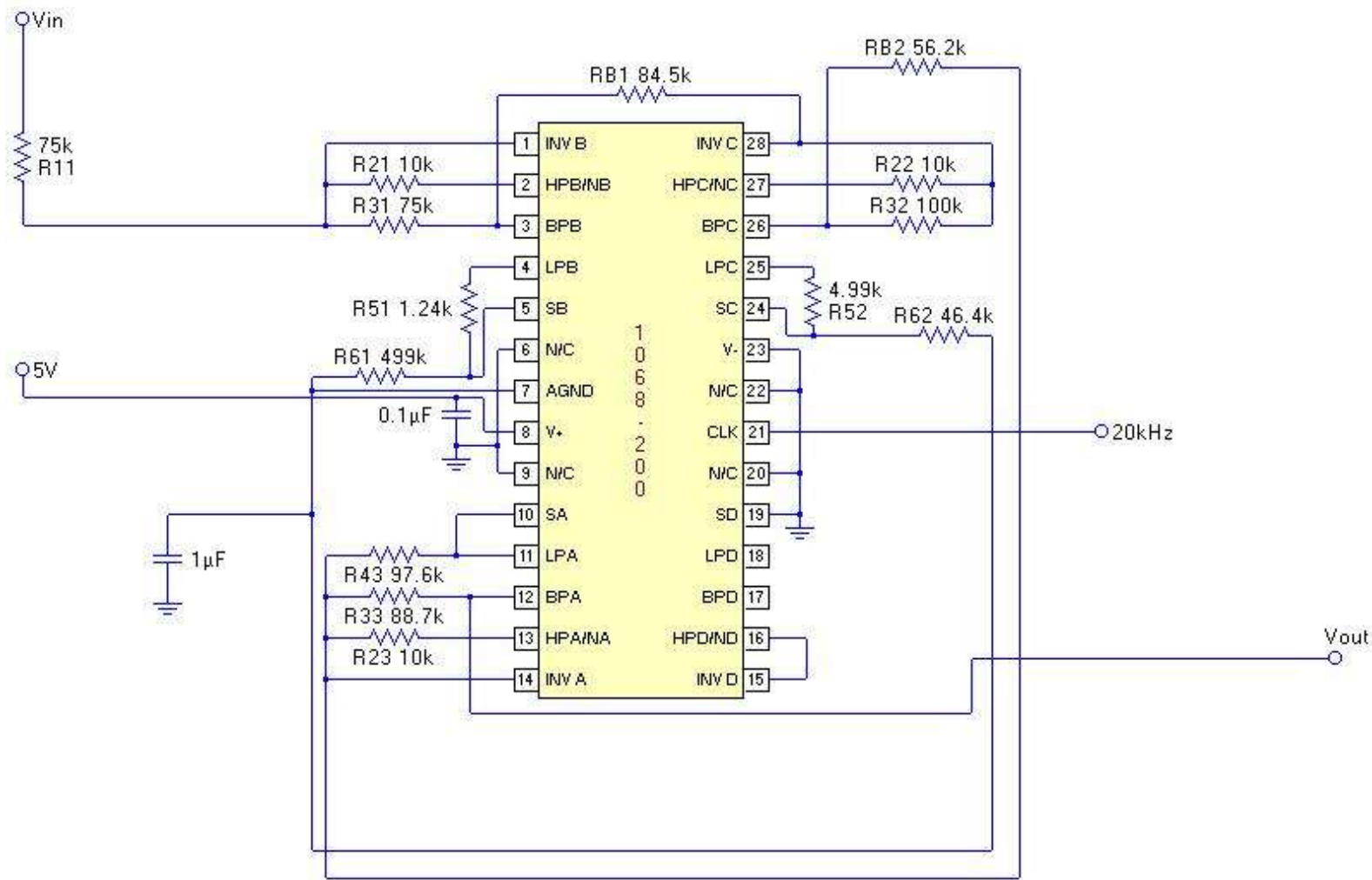




# Filtry C - przełączane

## LTC 1068 - Linear Technology

### Projektowania -FCAD





# Czujniki temperatury

## TMP 141 - Texas Instruments

### (Burr - Brown)

**TMP 141** - Digital out temperature sensor with Single-wire Sensor Path Bus

Układ TMP 141 jest czujnikiem temperatury z wyjściem cyfrowym, współpracującym z jednoprzewodową szyną transmisji danych.

### FEATURES

- SensorPath INTERFACE
- FOUR ADDRESSES
- RESOLUTION:  $+0.25^{\circ}\text{C}$  (10-bit)
- WIDE TEMPERATURE RANGE:  
 $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- LOW QUIESCENT CURRENT:  $110\mu\text{A}$  (typ)
- TEMPERATURE ACCURACY:  $\pm 2^{\circ}\text{C}$  (max)
- EXTENDED SUPPLY RANGE:  $+2.7\text{V}$  to  $+5.5\text{V}$
- MICRO-SIZE PACKAGES:  
SOT23-6 or MSOP-8

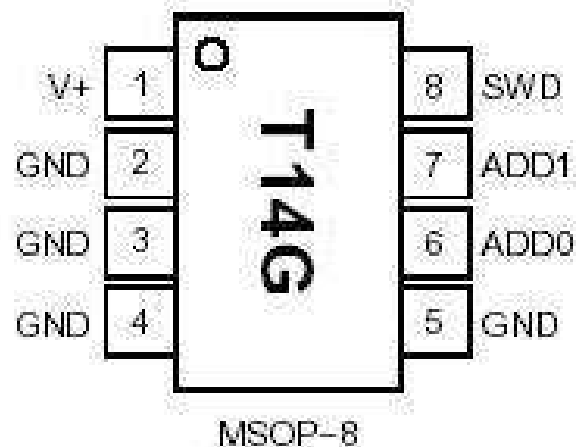
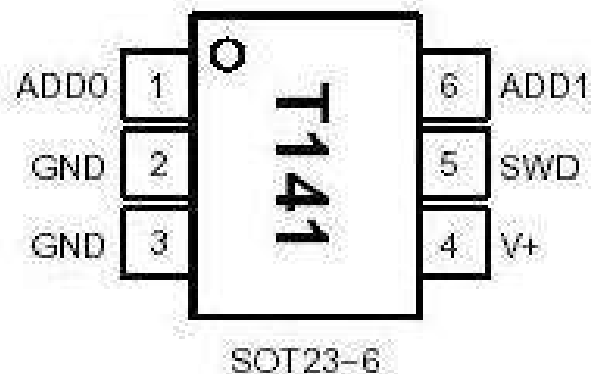
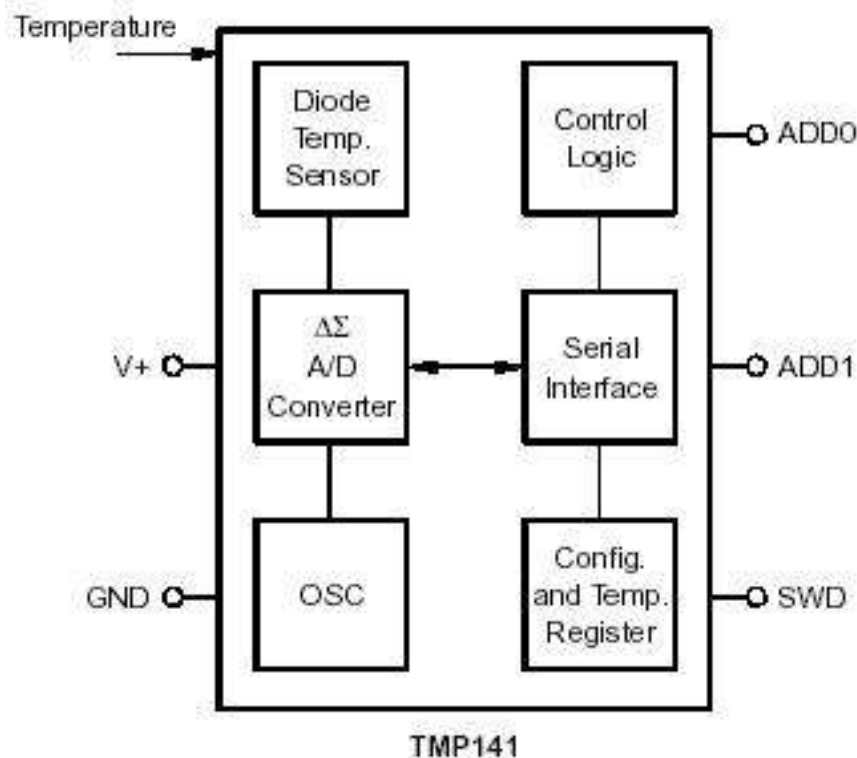
### APPLICATIONS

- MOTHERBOARDS
- VIDEO CARDS
- BASE STATIONS
- ROUTERS

# Czujniki temperatury

## TMP 141 - Texas Instruments

### (Burr - Brown)





# Czujniki temperature

## TMP 141 - Texas Instruments

### (Burr - Brown)

PARAMETER		CONDITIONS	TMP141			UNIT
			MIN	TYP	MAX	
<b>TEMPERATURE INPUT</b>						
Range			-40		+125	°C
Error	$T_{\text{ERROR}}$	$T = -25^{\circ}\text{C to } +85^{\circ}\text{C}$ $T = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		$\pm 0.2$	$\pm 2$	°C
vs Supply				$\pm 0.2$	$\pm 3$	°C/V
Resolution				10		Bits
				0.25		°C
Default Conversion Time	$t_{\text{CONV}}$	See Table 4 for conversion time settings.	162	190	218	ms
<b>DIGITAL INPUT/OUTPUT PINS (SWD and ADD pins)</b>						
Input/Output Capacitance	$C_{\text{IN/OUT}}$			3		pF
<b>SWD PIN</b>						
Input Leakage Current	$I_L$	$\text{GND} < V_{\text{IN}} < V_S$		0.005	10	μA
	$I_L$	$\text{GND} < V_{\text{IN}} < 5.5\text{V and } V_S = \text{GND/OPEN}$		0.005		μA
Input Logic Level Voltage (High)	$V_{\text{IH}}$	$V_S = 2.7\text{V to } 5.5\text{V}$	2.1 $0.6 \times V_S$		$V_S + 0.5$	V
Input Logic Level Voltage (Low)	$V_{\text{IL}}$	$V_S = 2.7\text{V to } 5.5\text{V}$	-0.5		0.8	V
Input Hysteresis	$V_{\text{HYST}}$	$V_S = 2.7\text{V to } 5.5\text{V}$	-0.5		$0.25 \times V_S$	V
Output Logic Level Voltage (Low)	$V_{\text{OL}}$	$I_{\text{OL}} = 4\text{mA}$ $I_{\text{OL}} = 50\mu\text{A}$		300	0.4	mV
Output OFF Current	$I_{\text{OH}}$				0.2	V
				0.005	10	μA
<b>ADD0 and ADD1 PINS</b>						
Input Leakage Current	$I_L$	$\text{GND} < V_{\text{IN}} < V_S$		0.005	10	μA
Input Logic Level Voltage (High)	$V_{\text{IH}}$		$0.9 \times V_S$		$V_S + 0.5$	V
Input Logic Level Voltage (Low)	$V_{\text{IL}}$		-0.5		$0.1 \times V_S$	V



# Czujniki temperature

## TMP 141 - Texas Instruments

### (Burr - Brown)

SensorPath CHARACTERISTICS						
SWD Fall Time	t <sub>f</sub>	R <sub>PULL-UP</sub> = 1.25kΩ ± 30%, C <sub>L</sub> = 400pF R <sub>PULL-UP</sub> = 1.25kΩ ± 30%, C <sub>L</sub> = 400pF Bus at High Level		300	ns	
SWD Rise Time	t <sub>r</sub>			1000	ns	
Min. Inactive Time Between SWD Signals	t <sub>INACT</sub>		11		μs	
Master or TMP141 Reset Drive Time	t <sub>RST</sub>		354		μs	
TMP141 Detects Bus Activity	t <sub>SFEdet</sub>			9.6	μs	
Master Drive Time						
Data Bit 0 Write, Data Bit 0 Read	t <sub>Mtr0</sub>		11.8	17	μs	
Data Bit 1 Write	t <sub>Mtr1</sub>		35.4	48.9	μs	
Start Bit	t <sub>MtrS</sub>		80	109	μs	
TMP141 Drive Time						
Data Bit 0–1 Read	t <sub>SLout1</sub>		28.3	38.3	μs	
Attention Request	t <sub>SLoutA</sub>		165	228	μs	
Reset	t <sub>RST_MAX</sub>	After V <sub>S</sub> is Above 2.6V		95	500	ms
POWER SUPPLY						
Specified Voltage Range			3.0	3.6	V	
Operating Voltage Range			2.7	5.5	V	
Quiescent Current	I <sub>Q</sub>	Standby		80	μA	
		While Converting <sup>(1)</sup>		110	μA	
Power-On Reset Voltage			1.5	2.6	V	
TEMPERATURE RANGE						
Specified Range			–40	+125	°C	
Operating Range			–55	+127	°C	
Storage Range			–60	+150	°C	
Thermal Resistance	θ <sub>JA</sub>					
MSOP-8				150	°C/W	
SOT23-6				200	°C/W	

# Czujniki temperature

## TMP 141 - Texas Instruments (Burr - Brown)

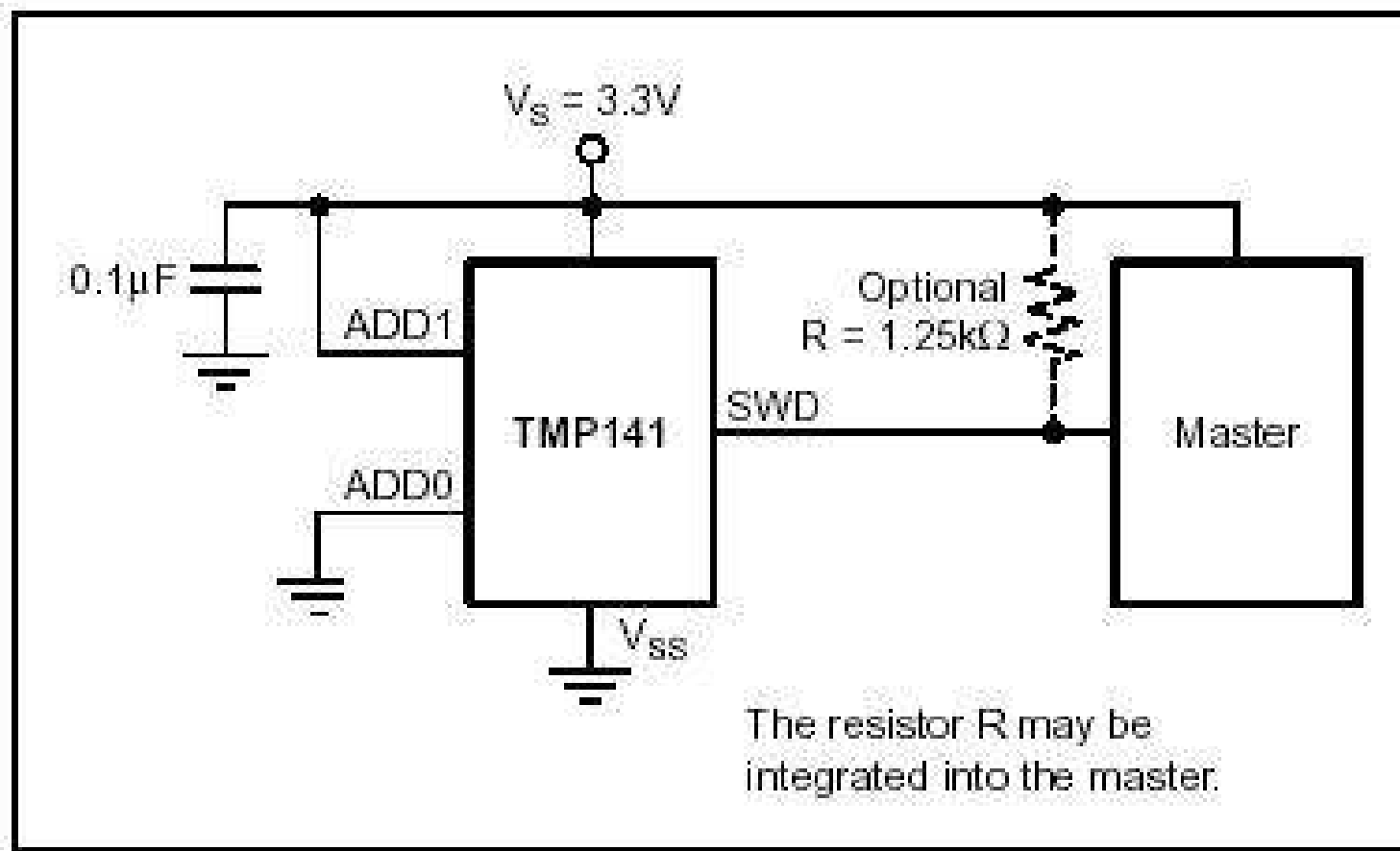


Figure 3. Typical Connections of the TMP141



# Nadajniki pętli prądowych XTR 105 - Texas Instruments (Burr - Brown)

**XTR 105** - 4-20 mA Current transmitter with Sensor Excitation and Linearization

Układ XTR 105 jest nadajnikiem pętli prądowej 4-20 mA z wbudowanymi układami zasilania i linearyzacji współpracującego z nim czujnika temperatury.

## FEATURES

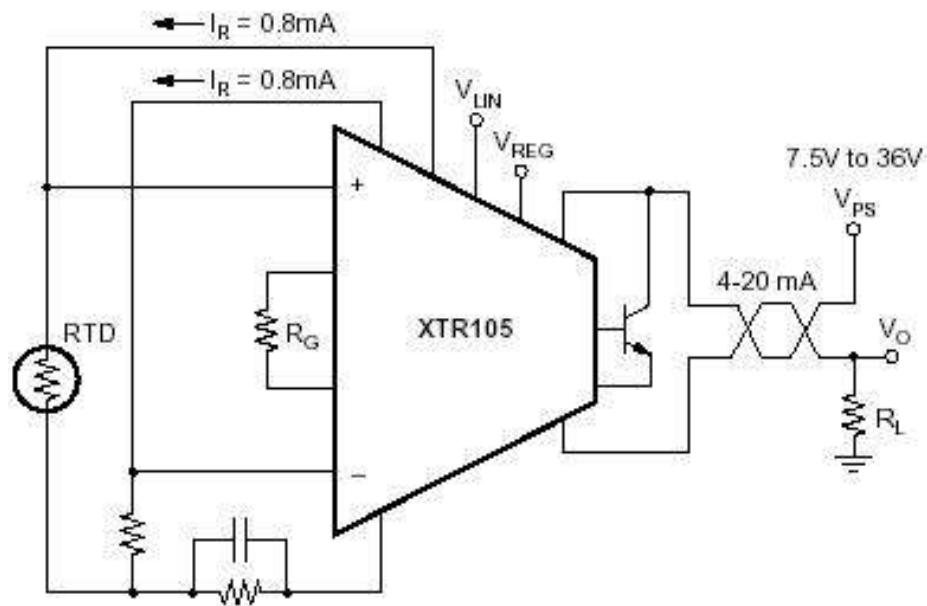
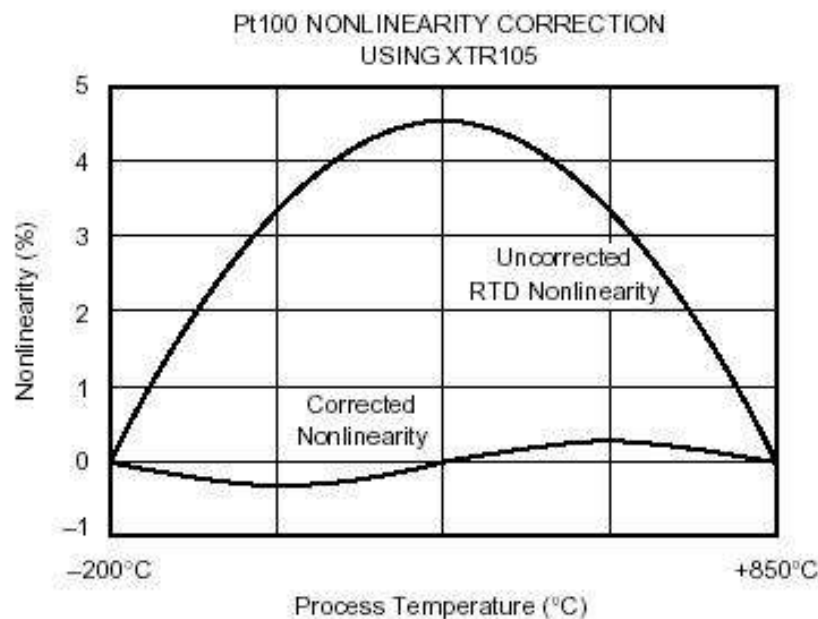
- LOW UNADJUSTED ERROR
- TWO PRECISION CURRENT SOURCES: 800 $\mu$ A each
- LINEARIZATION
- 2- OR 3-WIRE RTD OPERATION
- LOW OFFSET DRIFT: 0.4 $\mu$ V/ $^{\circ}$ C
- LOW OUTPUT CURRENT NOISE: 30nA<sub>pp</sub>
- HIGH PSR: 110dB minimum
- HIGH CMR: 86dB minimum
- WIDE SUPPLY RANGE: 7.5V to 36V
- DIP-14 AND SO-14 PACKAGES

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA REMOTE DATA ACQUISITION
- REMOTE TEMPERATURE AND PRESSURE TRANSDUCERS



# Nadajniki pętli prądowych XTR 105 - Texas Instruments (Burr - Brown)





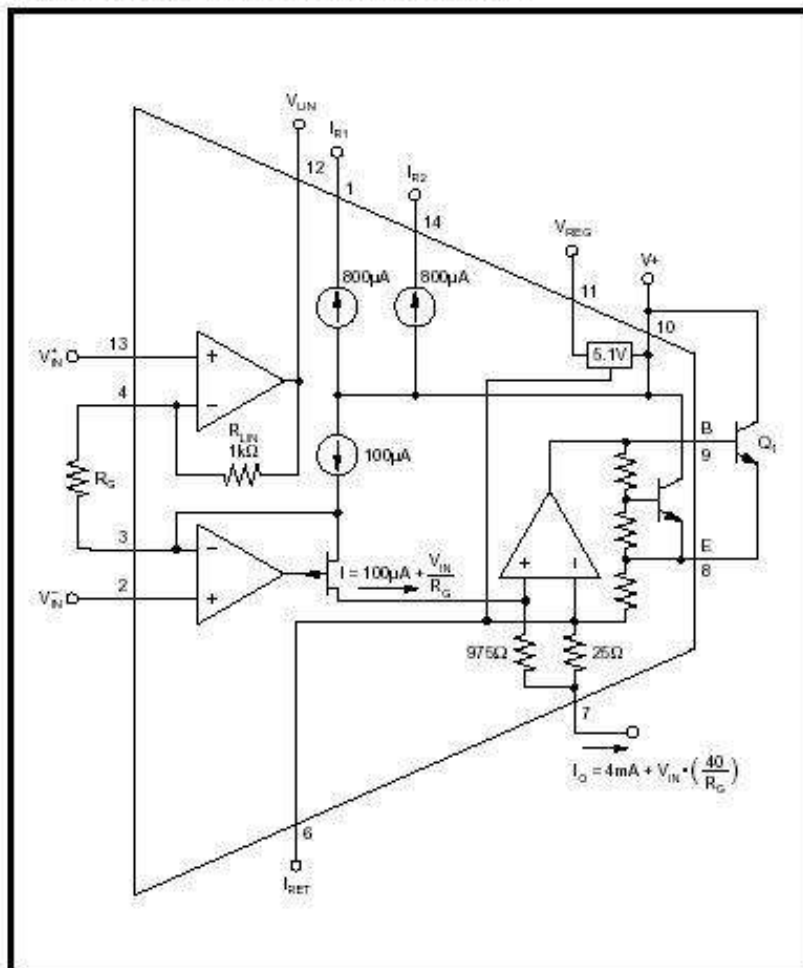


# Nadajniki pętli prądowych

## XTR 105 - Texas Instruments

### (Burr - Brown)

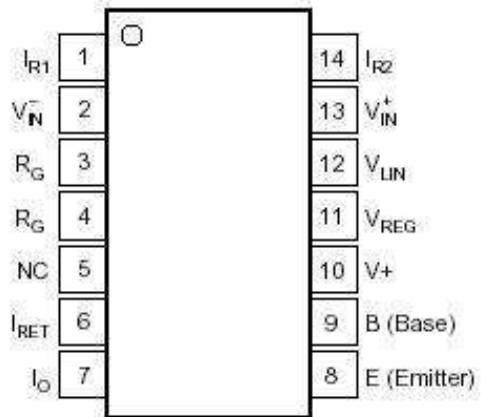
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Top View

DIP and SO



NC = No Internal Connection



# Nadajniki pętli prądowych

## XTR 105 - Texas Instruments

### (Burr - Brown)

PARAMETER	CONDITIONS	XTR105P, U			XTR105PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT</b>								
Output Current Equation		$I_O = V_{IN} \cdot (40/R_G) + 4\text{mA}$ , $V_{IN}$ in Volts, $R_G$ in $\Omega$						A
Output Current, Specified Range		4		20	*		*	mA
Over-Scale Limit		24	27	30	*	*	*	mA
Under-Scale Limit	$I_{REG} = 0V$	1.8	2.2	2.6	*	*	*	mA
<b>ZERO OUTPUT<sup>(1)</sup></b>	$V_{IN} = 0V$ , $R_G = \infty$		4			*		mA
Initial Error			$\pm 5$	$\pm 25$		*	$\pm 50$	$\mu A$
vs Temperature			$\pm 0.07$	$\pm 0.5$		*	$\pm 0.9$	$\mu A/^{\circ}C$
vs Supply Voltage, $V_+$	$V_+ = 7.5V$ to $36V$		0.04	0.2		*	*	$\mu A/V$
vs Common-Mode Voltage	$V_{CM} = 1.25V$ to $3.5V^{(2)}$		0.02			*		$\mu A/V$
vs $V_{REG}$ Output Current			0.3			*		$\mu A/mA$
Noise, 0.1Hz to 10Hz			0.03			*		$\mu A_{PP}$
<b>SPAN</b>								
Span Equation (transconductance)			$S = 40/R_G$			*		A/V
Initial Error <sup>(3)</sup>	Full-Scale ( $V_N$ ) = 50mV		$\pm 0.05$	$\pm 0.2$		*	$\pm 0.4$	%
vs Temperature <sup>(3)</sup>			$\pm 3$	$\pm 25$		*	*	ppm/ $^{\circ}C$
Nonlinearity, Ideal Input <sup>(4)</sup>	Full-Scale ( $V_N$ ) = 50mV		0.003	0.01		*	*	%
<b>INPUT<sup>(5)</sup></b>								
Offset Voltage	$V_{CM} = 2V$		$\pm 50$	$\pm 100$		*	$\pm 250$	$\mu V$
vs Temperature			$\pm 0.4$	$\pm 1.5$		*	$\pm 3$	$\mu V/^{\circ}C$
vs Supply Voltage, $V_+$	$V_+ = 7.5V$ to $36V$		$\pm 0.3$	$\pm 3$		*	*	$\mu V/V$
vs Common-Mode Voltage, RTI (CMRR)	$V_{CM} = 1.25V$ to $3.5V^{(2)}$		$\pm 10$	$\pm 50$		*	$\pm 100$	$\mu V/V$
Common-Mode Input Range <sup>(2)</sup>		1.25		3.5	*		*	V
Input Bias Current			5	25		*	50	nA
vs Temperature			20			*		pA/ $^{\circ}C$
Input Offset Current			$\pm 0.2$	$\pm 3$		*	$\pm 10$	nA
vs Temperature			5			*		pA/ $^{\circ}C$
Impedance, Differential			$0.1 \parallel 1$			*		G $\Omega \parallel$ pF
Common-Mode			$5 \parallel 10$			*		G $\Omega \parallel$ pF
Noise, 0.1Hz to 10Hz			0.6			*		$\mu V_{PP}$

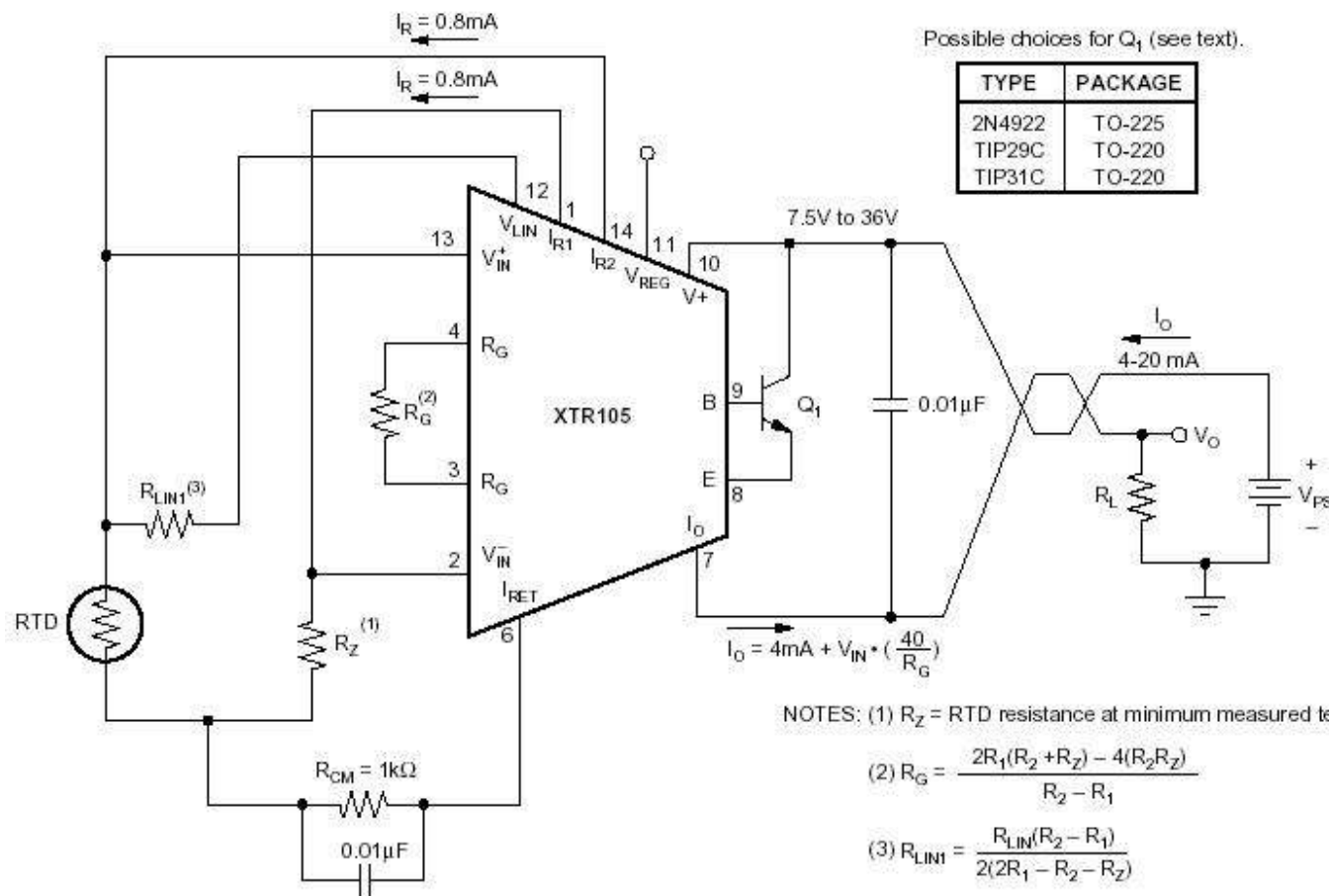


# Nadajniki pętli prądowych XTR 105 - Texas Instruments (Burr - Brown)

<b>CURRENT SOURCES</b>	$V_O = 2V^{(6)}$		800			*		$\mu A$
Current			$\pm 0.05$	$\pm 0.2$		*	$\pm 0.4$	%
Accuracy			$\pm 15$	$\pm 35$		*	$\pm 75$	ppm/ $^{\circ}C$
vs Temperature	$V+ = 7.5V$ to $36V$		$\pm 10$	$\pm 25$		*	*	ppm/V
vs Power Supply, V+			$\pm 0.02$	$\pm 0.1$		*	$\pm 0.2$	%
Matching			$\pm 3$	$\pm 15$		*	$\pm 30$	ppm/ $^{\circ}C$
vs Temperature	$V+ = 7.5V$ to $36V$		1	10		*	*	ppm/V
vs Power Supply, V+			$(V+) - 3$	$(V+) - 2.5$	*	*		V
Compliance Voltage, Positive		0	-0.2		*	*		V
Negative <sup>(2)</sup>			150			*		M $\Omega$
Output Impedance			0.003			*		$\mu A_{pp}$
Noise, 0.1Hz to 10Hz								
<b>V<sub>REG</sub><sup>(2)</sup></b>			5.1			*		V
Accuracy			$\pm 0.02$	$\pm 0.1$		*	*	V
vs Temperature			$\pm 0.2$			*		mV/ $^{\circ}C$
vs Supply Voltage, V+			1			*		mV/V
Output Current			$\pm 1$			*		mA
Output Impedance			75			*		$\Omega$
<b>LINEARIZATION</b>								
R <sub>UN</sub> (internal)			1			*		k $\Omega$
Accuracy			$\pm 0.2$	$\pm 0.5$		*	$\pm 1$	%
vs Temperature			$\pm 25$	$\pm 100$		*	*	ppm/ $^{\circ}C$
<b>POWER SUPPLY</b>								
Specified			+24			*		V
Voltage Range		+7.5		+36	*	*	*	V
<b>TEMPERATURE RANGE</b>								
Specification, T <sub>MIN</sub> to T <sub>MAX</sub>		-40		+85	*		*	$^{\circ}C$
Operating		-55		+125	*		*	$^{\circ}C$
Storage		-55		+125	*		*	$^{\circ}C$
Thermal Resistance, $\theta_{JA}$								
DIP-14			80			*		$^{\circ}C/W$
SO-14 Surface-Mount			100			*		$^{\circ}C/W$



# Nadajniki pętli prądowych XTR 105 - Texas Instruments (Burr - Brown)



where  $R_1$  = RTD Resistance at  $(T_{MIN} + T_{MAX})/2$

$R_2$  = RTD Resistance at  $T_{MAX}$

$R_{LIN} = 1k\Omega$  (Internal)



# Nadajniki pętli prądowych XTR 105 - Texas Instruments (Burr - Brown)

MEASUREMENT TEMPERATURE SPAN  $\Delta T$  (°C)

T <sub>MIN</sub>	100°C	200°C	300°C	400°C	500°C	600°C	700°C	800°C	900°C	1000°C
-200°C	18.7/86.6 15000 16500	18.7/169 9760 11500	18.7/255 8060 10000	18.7/340 6650 8870	18.7/422 5620 7870	18.7/511 4750 7150	18.7/590 4020 6420	18.7/665 3480 5900	18.7/750 3090 5360	18.7/845 2740 4990
-100°C	60.4/80.6 27400 29400	60.4/162 15400 17800	60.4/243 10500 13000	60.4/324 7870 10200	60.4/402 6040 8660	60.4/487 4990 7500	60.4/562 4220 6490	60.4/649 3570 5900	60.4/732 3090 5360	
0°C	100/78.7 33200 35700	100/158 16200 18700	100/237 10500 13000	100/316 7680 10000	100/392 6040 8250	100/475 4870 7150	100/549 4020 6340	100/634 3480 5620		
100°C	137/75 31600 34000	137/150 15400 17800	137/226 10200 12400	137/301 7500 9760	137/383 5760 8060	137/453 4750 6810	137/536 3920 6040			
200°C	174/73.2 30900 33200	174/147 15000 17400	174/221 9760 12100	174/294 7150 9310	174/365 5620 7680	174/442 4530 6490				
300°C	210/71.5 30100 32400	210/143 14700 16500	210/215 9530 11500	210/287 6980 8870	210/357 5360 7320					
400°C	249/68.1 28700 30900	249/137 14000 16200	249/205 9090 11000	249/274 6650 8450						
500°C	280/66.5 28000 30100	280/133 13700 15400	280/200 8870 10500							
600°C	316/64.9 26700 28700	313/130 13000 14700								
700°C	348/61.9 26100 27400									
800°C	374/60.4 24900 26700									

$R_Z/R_G$   
 $R_{LIN1}$   
 $R_{LIN2}$

NOTE: The values listed in this table are 1% resistors (in  $\Omega$ ).  
Exact values may be calculated from the following equations:

$R_Z$  = RTD resistance at minimum measured temperature.

$$R_G = \frac{2(R_Z - R_1)(R_1 - R_Z)}{(R_2 - R_1)}$$

$$R_{LIN1} = \frac{R_{LIN}(R_2 - R_1)}{2(R_1 - R_2 - R_Z)}$$

$$R_{LIN2} = \frac{(R_{LIN} + R_G)(R_2 - R_1)}{2(R_1 - R_2 - R_Z)}$$

where:  $R_1$  = RTD resistance at  $(T_{MIN} + T_{MAX})/2$

$R_2$  = RTD resistance at  $T_{MAX}$

$R_{LIN}$  = 1k $\Omega$  (Internal)



# Mnożniki

## AD 633 - Analog Devices

### AD 633 - Low Cost Analog Multiplier

Układ AD 633 jest tanim mnożnikiem analogowym.

#### FEATURES

- Four-Quadrant Multiplication
- Low Cost 8-Lead Package
- Complete—No External Components Required
- Laser-Trimmed Accuracy and Stability
- Total Error Within 2% of FS
- Differential High Impedance X and Y Inputs
- High Impedance Unity-Gain Summing Input
- Laser-Trimmed 10 V Scaling Reference

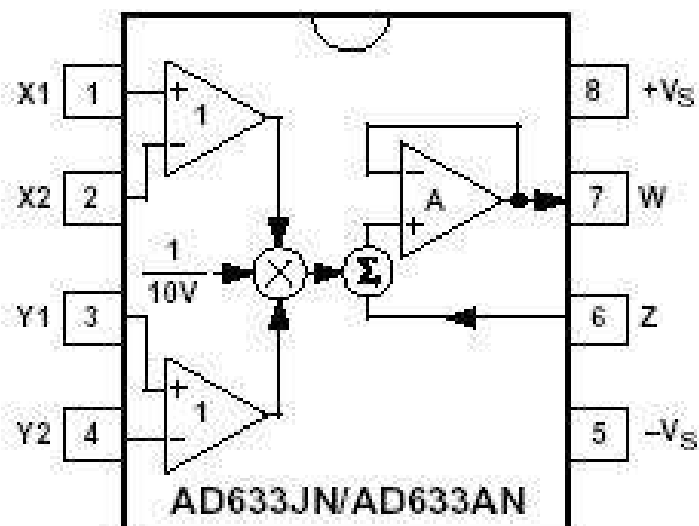
#### APPLICATIONS

- Multiplication, Division, Squaring
- Modulation/Demodulation, Phase Detection
- Voltage-Controlled Amplifiers/Attenuators/Filters

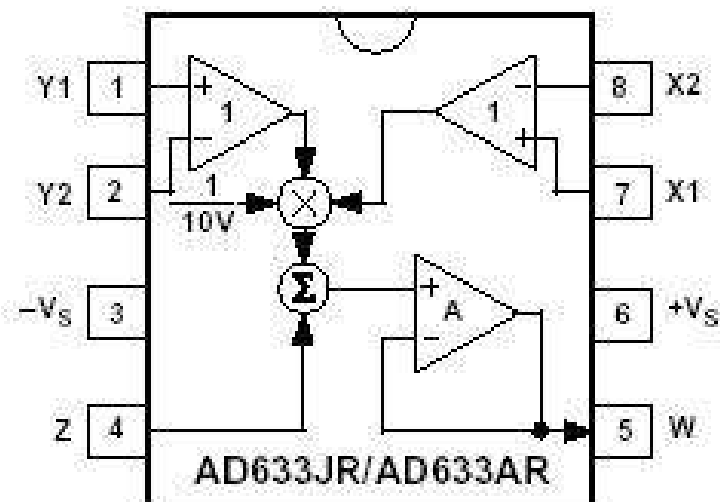
# Mnożniki

## AD 633 - Analog Devices

**CONNECTION DIAGRAMS**  
8-Lead Plastic DIP (N) Package



8-Lead Plastic SOIC (SO-8) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$





# Mnożniki

## AD 633 - Analog Devices

Model		AD633J, AD633A			
TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10 V} + Z$			
Parameter	Conditions	Min	Typ	Max	Unit
<b>MULTIPLIER PERFORMANCE</b>					
Total Error	$-10 V \leq X, Y \leq +10 V$		$\pm 1$	$\pm 2$	% Full Scale
$T_{MIN}$ to $T_{MAX}$			$\pm 3$		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		$\pm 0.25\%$		% Full Scale
Supply Rejection	$V_S = \pm 14 V$ to $\pm 16 V$		$\pm 0.01$		% Full Scale
Nonlinearity, X	$X = \pm 10 V, Y = +10 V$		$\pm 0.4$	$\pm 1$	% Full Scale
Nonlinearity, Y	$Y = \pm 10 V, X = +10 V$		$\pm 0.1$	$\pm 0.4$	% Full Scale
X Feedthrough	Y Nulled, $X = \pm 10 V$		$\pm 0.3$	$\pm 1$	% Full Scale
Y Feedthrough	X Nulled, $Y = \pm 10 V$		$\pm 0.1$	$\pm 0.4$	% Full Scale
Output Offset Voltage			$\pm 5$	$\pm 50$	mV
<b>DYNAMICS</b>					
Small Signal BW	$V_O = 0.1 V$ rms		1		MHz
Slew Rate	$V_O = 20 V$ p-p		20		V/ $\mu$ s
Settling Time to 1%	$\Delta V_O = 20 V$		2		$\mu$ s
<b>OUTPUT NOISE</b>					
Spectral Density			0.8		$\mu V/\sqrt{Hz}$
Wideband Noise	$f = 10 Hz$ to $5 MHz$		1		mV rms
	$f = 10 Hz$ to $10 kHz$		90		$\mu V$ rms
<b>OUTPUT</b>					
Output Voltage Swing		$\pm 11$			V
Short Circuit Current	$R_L = 0 \Omega$		30	40	mA
<b>INPUT AMPLIFIERS</b>					
Signal Voltage Range	Differential	$\pm 10$			V
	Common Mode	$\pm 10$			V
Offset Voltage X, Y			$\pm 5$	$\pm 30$	mV
CMRR X, Y	$V_{CM} = \pm 10 V, f = 50 Hz$	60	80		dB
Bias Current X, Y, Z			0.8	2.0	$\mu A$
Differential Resistance			10		M $\Omega$



# Mnożniki

## AD 633 - Analog Devices

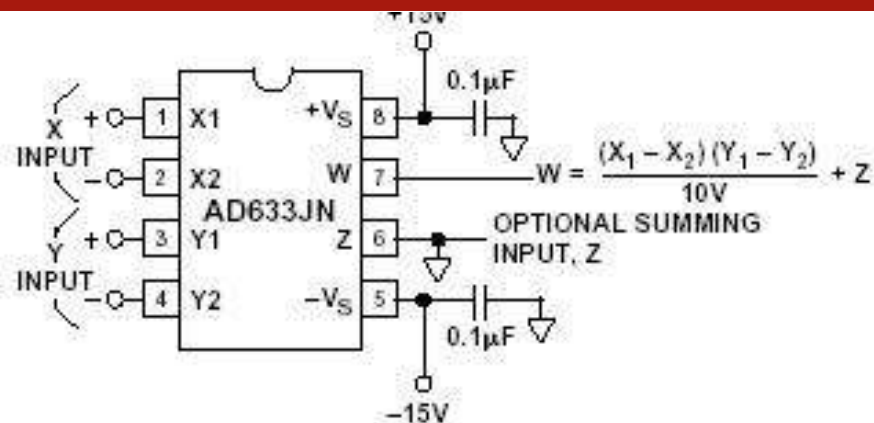


Figure 3. Basic Multiplier Connections

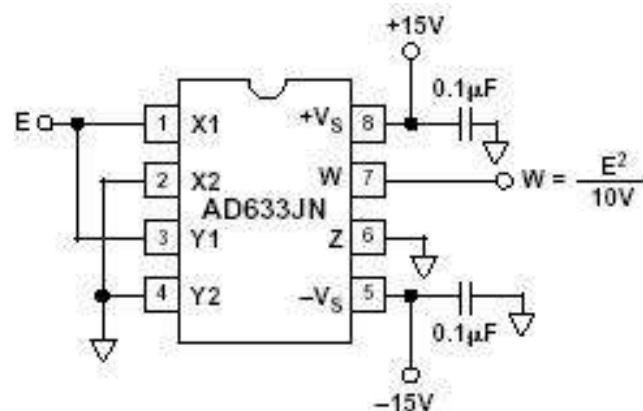


Figure 4. Connections for Squaring

# Mnożniki

## AD 633 - Analog Devices

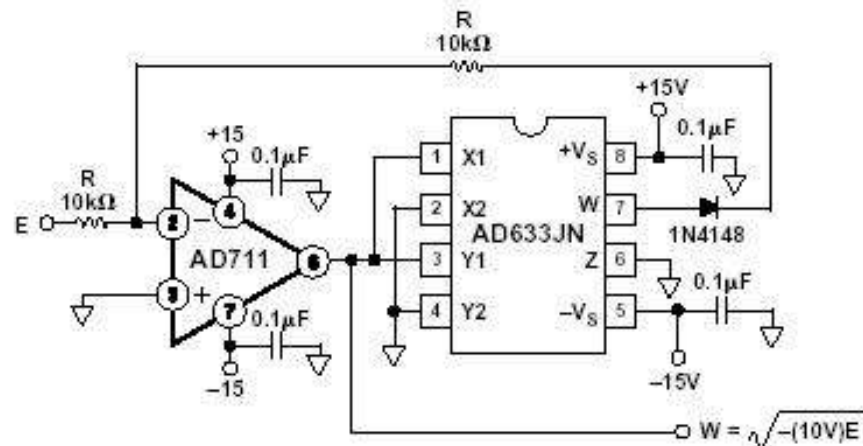


Figure 6. Connections for Square Rooting

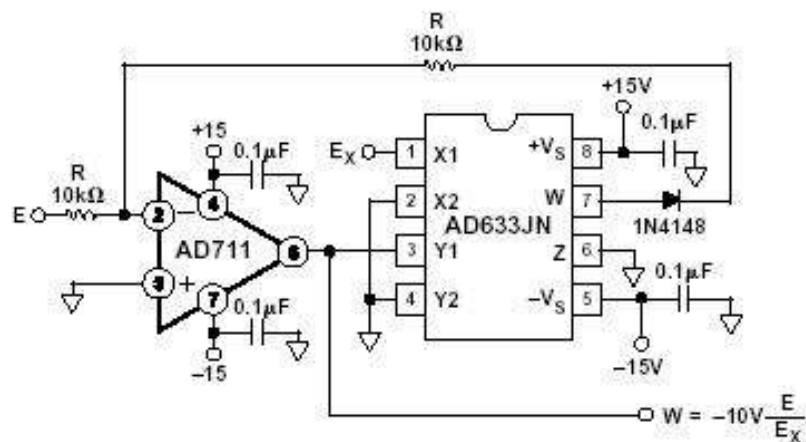
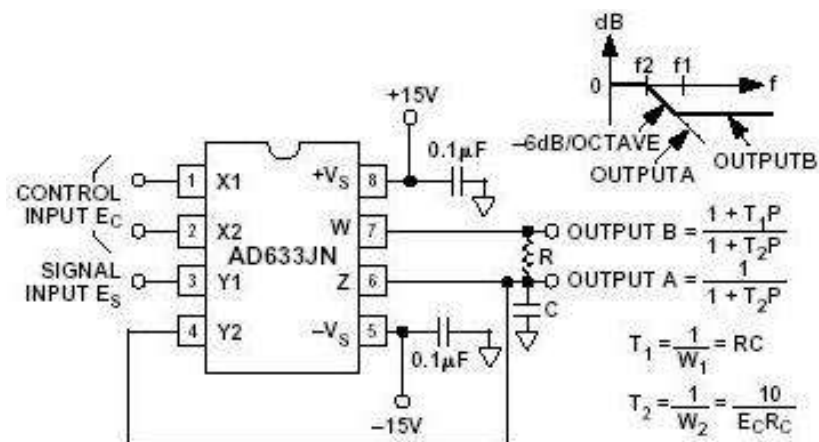


Figure 7. Connections for Division

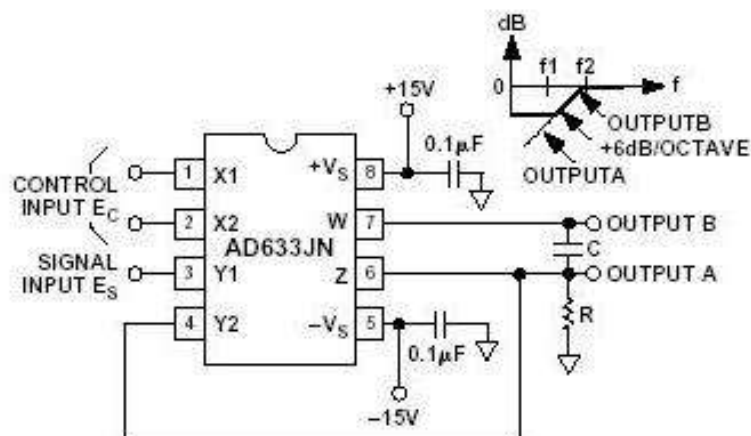
# Mnożniki

## AD 633 - Analog Devices



$$f_1 = \frac{1}{2\pi RC}$$

$$f_2 = \frac{E_C}{(20V)\pi RC}$$



# Generatory przebiegów okresowych

## MAX 038 - MAXIM

**MAX 038** - High frequency waveform generator.

Układ MAX 038 jest scalonym generatorem przebiegów okresowych wielkiej częstotliwości.

### ***Features***

- ◆ 0.1Hz to 20MHz Operating Frequency Range
- ◆ Triangle, Sawtooth, Sine, Square, and Pulse Waveforms
- ◆ Independent Frequency and Duty-Cycle Adjustments
- ◆ 350 to 1 Frequency Sweep Range
- ◆ 15% to 85% Variable Duty Cycle
- ◆ Low-Impedance Output Buffer:  $0.1\Omega$
- ◆ Low-Distortion Sine Wave: 0.75%
- ◆ Low 200ppm/°C Temperature Drift



# Generatory przebiegów okresowych MAX 038 - MAXIM

## ***Applications***

Precision Function Generators

Voltage-Controlled Oscillators

Frequency Modulators

Pulse-Width Modulators

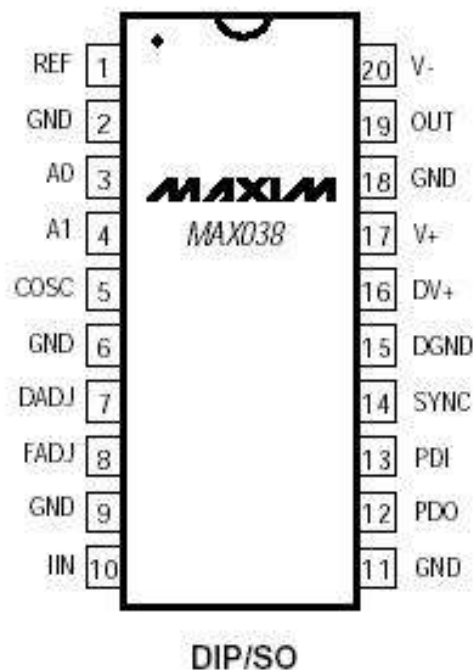
Phase-Locked Loops

Frequency Synthesizer

FSK Generator—Sine and Square Waves

# Generatory przebiegów okresowych

## MAX 038 - MAXIM



PIN	NAME	FUNCTION
1	REF	2.50V bandgap voltage reference output
2, 6, 9, 11, 18	GND	Ground*
3	AO	Waveform selection input; TTL/CMOS compatible
4	A1	Waveform selection input; TTL/CMOS compatible
5	COSC	External capacitor connection
7	DADJ	Duty-cycle adjust input
8	FADJ	Frequency adjust input
10	IIN	Current input for frequency control
12	PDO	Phase detector output. Connect to GND if phase detector is not used.
13	PDI	Phase detector reference clock input. Connect to GND if phase detector is not used.
14	SYNC	TTL/CMOS-compatible output, referenced between DGND and DV+. Permits the internal oscillator to be synchronized with an external signal. Leave open if unused.
15	DGND	Digital ground
16	DV+	Digital +5V supply input. Can be left open if SYNC is not used.
17	V+	+5V supply input
19	OUT	Sine, square, or triangle output
20	V-	-5V supply input



# Generatory przebiegów okresowych

## MAX 038 - MAXIM

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY CHARACTERISTICS						
Maximum Operating Frequency	F <sub>o</sub>	15pCF ≤ 15pF, I <sub>IN</sub> = 500μA	20.0	40.0		MHz
Frequency Programming Current	I <sub>IN</sub>	V <sub>FADJ</sub> = 0V	2.50		750	μA
		V <sub>FADJ</sub> = -3V	1.25		375	
IIN Offset Voltage	V <sub>IN</sub>			±1.0	±2.0	mV
Frequency Temperature Coefficient	ΔF <sub>o</sub> /°C	V <sub>FADJ</sub> = 0V		600		ppm/°C
	F <sub>o</sub> /°C	V <sub>FADJ</sub> = -3V		200		
Frequency Power-Supply Rejection	$\frac{(\Delta F_o/F_o)}{\Delta V+}$	V <sub>-</sub> = -5V, V <sub>+</sub> = 4.75V to 5.25V		±0.4	±2.00	%V
	$\frac{(\Delta F_o/F_o)}{\Delta V-}$	V <sub>+</sub> = 5V, V <sub>-</sub> = -4.75V to -5.25V		±0.2	±1.00	
OUTPUT AMPLIFIER (applies to all waveforms)						
Output Peak-to-Peak Symmetry	V <sub>OUT</sub>			±4		mV
Output Resistance	R <sub>OUT</sub>			0.1	0.2	Ω
Output Short-Circuit Current	I <sub>OUT</sub>	Short circuit to GND		40		mA
SQUARE-WAVE OUTPUT (R <sub>L</sub> = 100Ω)						
Amplitude	V <sub>OUT</sub>		1.9	2.0	2.1	V <sub>p-p</sub>
Rise Time	t <sub>R</sub>	10% to 90%		12		ns
Fall Time	t <sub>F</sub>	90% to 10%		12		ns
Duty Cycle	dc	V <sub>DADJ</sub> = 0V, dc = t <sub>ON</sub> /t × 100%	47	50	53	%





# Generatory przebiegów okresowych

## MAX 038 - MAXIM

TRIANGLE-WAVE OUTPUT (R <sub>L</sub> = 100Ω)						
Amplitude	V <sub>OUT</sub>		1.9	2.0	2.1	V <sub>P-P</sub>
Nonlinearity		F <sub>O</sub> = 100kHz, 5% to 95%		0.5		%
Duty Cycle	dc	V <sub>DADJ</sub> = 0V (Note 1)	47	50	53	%
SINE-WAVE OUTPUT (R <sub>L</sub> = 100Ω)						
Amplitude	V <sub>OUT</sub>		1.9	2.0	2.1	V <sub>P-P</sub>
Total Harmonic Distortion	THD	Duty cycle adjusted to 50%		0.75		%
		Duty cycle unadjusted		1.50		
SYNC OUTPUT						
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 3.2mA		0.3	0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 400μA	2.8	3.5		V
Rise Time	t <sub>R</sub>	10% to 90%, R <sub>L</sub> = 3kΩ, C <sub>L</sub> = 15pF		10		ns
Fall Time	t <sub>F</sub>	90% to 10%, R <sub>L</sub> = 3kΩ, C <sub>L</sub> = 15pF		10		ns
Duty Cycle	dc <sub>SYNC</sub>			50		%
DUTY-CYCLE ADJUSTMENT (DADJ)						
DADJ Input Current	I <sub>DADJ</sub>		190	250	320	μA
DADJ Voltage Range	V <sub>DADJ</sub>			±2.3		V
Duty-Cycle Adjustment Range	dc	-2.3V ≤ V <sub>DADJ</sub> ≤ 2.3V	15		85	%
DADJ Nonlinearity	dc/V <sub>FADJ</sub>	-2V ≤ V <sub>DADJ</sub> ≤ 2V		2	4	%
Change in Output Frequency with DADJ	F <sub>O</sub> /V <sub>DADJ</sub>	-2V ≤ V <sub>DADJ</sub> ≤ 2V		±2.5	±8	%
Maximum DADJ Modulating Frequency	F <sub>DC</sub>			2		MHz





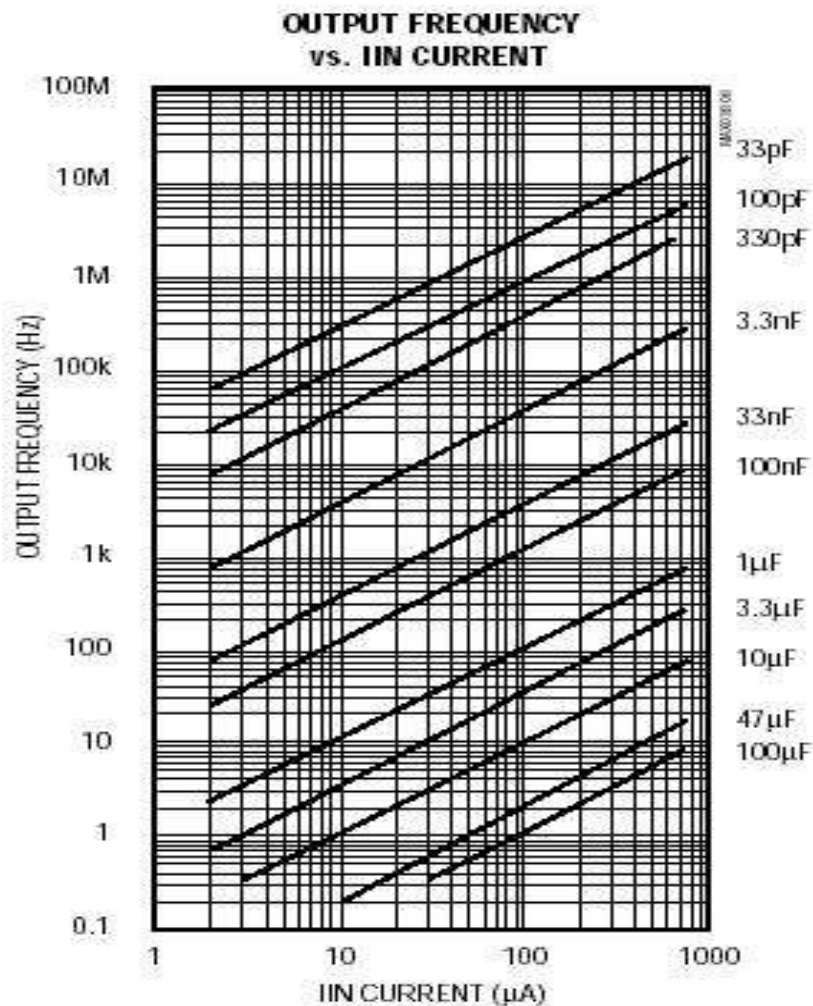
# Generatory przebiegów okresowych

## MAX 038 - MAXIM

FREQUENCY ADJUSTMENT (FADJ)						
FADJ Input Current	$I_{FADJ}$		190	250	320	$\mu A$
FADJ Voltage Range	$V_{FADJ}$		$\pm 2.4$			V
Frequency Sweep Range	$F_o$	$-2.4V \leq V_{FADJ} \leq 2.4V$	$\pm 70$			%
FM Nonlinearity with FADJ	$F_o/V_{FADJ}$	$-2V \leq V_{FADJ} \leq 2V$	$\pm 0.2$			%
Change in Duty Cycle with FADJ	$dc/V_{FADJ}$	$-2V \leq V_{FADJ} \leq 2V$	$\pm 2$			%
Maximum FADJ Modulating Frequency	$F_F$		2			MHz
VOLTAGE REFERENCE						
Output Voltage	$V_{REF}$	$I_{REF} = 0$	2.48	2.50	2.52	V
Temperature Coefficient	$V_{REF}/^{\circ}C$		20			ppm/ $^{\circ}C$
Load Regulation	$V_{REF}/I_{REF}$	$0mA \leq I_{REF} \leq 4mA$ (source)	1			mV/mA
		$-100\mu A \leq I_{REF} \leq 0\mu A$ (sink)	1			
Line Regulation	$V_{REF}/V_+$	$4.75V \leq V_+ \leq 5.25V$ (Note 2)	1			mV/V
LOGIC INPUTS (A0, A1, PDI)						
Input Low Voltage	$V_{IL}$		0.8			V
Input High Voltage	$V_{IH}$		2.4			V
Input Current (A0, A1)	$I_{IL}, I_{IH}$	$V_{A0}, V_{A1} = V_{IL}, V_{IH}$	$\pm 5$			$\mu A$
Input Current (PDI)	$I_{IL}, I_{IH}$	$V_{PDI} = V_{IL}, V_{IH}$	$\pm 25$			$\mu A$
POWER SUPPLY						
Positive Supply Voltage	$V_+$		4.75	5.25		V
SYNC Supply Voltage	$DV_+$		4.75	5.25		V
Negative Supply Voltage	$V_-$		-4.75	-5.25		V
Positive Supply Current	$I_+$		35		45	mA
SYNC Supply Current	$IDV_+$		1		2	mA
Negative Supply Current	$I_-$		45		55	mA



# Generatory przebiegów okresowych MAX 038 - MAXIM



# Generatory przebiegów okresowych MAX 038 - MAXIM

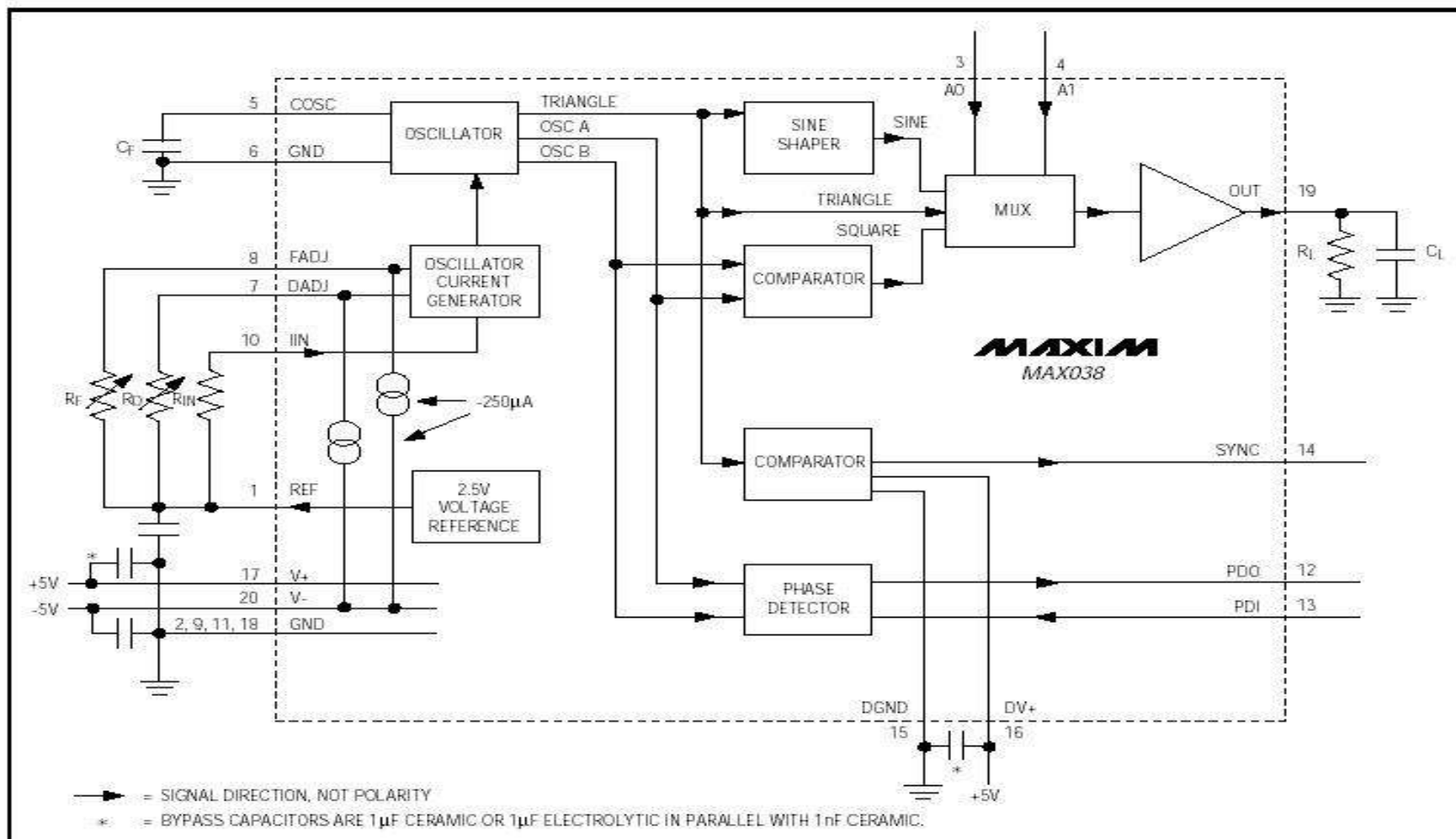


Figure 1. Block Diagram and Basic Operating Circuit

# Generatory przebiegów okresowych

## MAX 038 - MAXIM

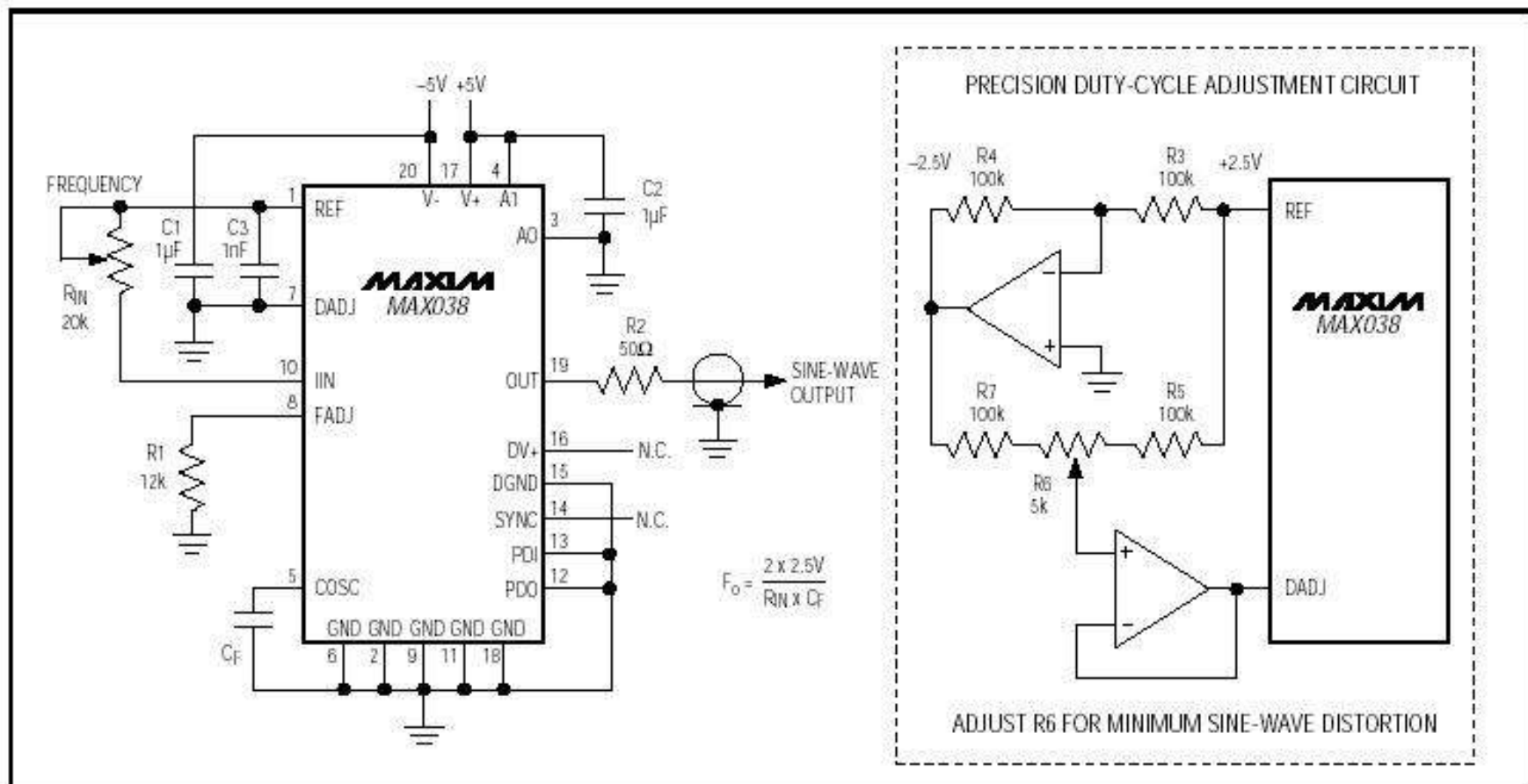


Figure 2. Operating Circuit with Sine-Wave Output and 50% Duty Cycle; SYNC and FADJ Disabled

# Generatory przebiegów okresowych

## MAX 038 - MAXIM

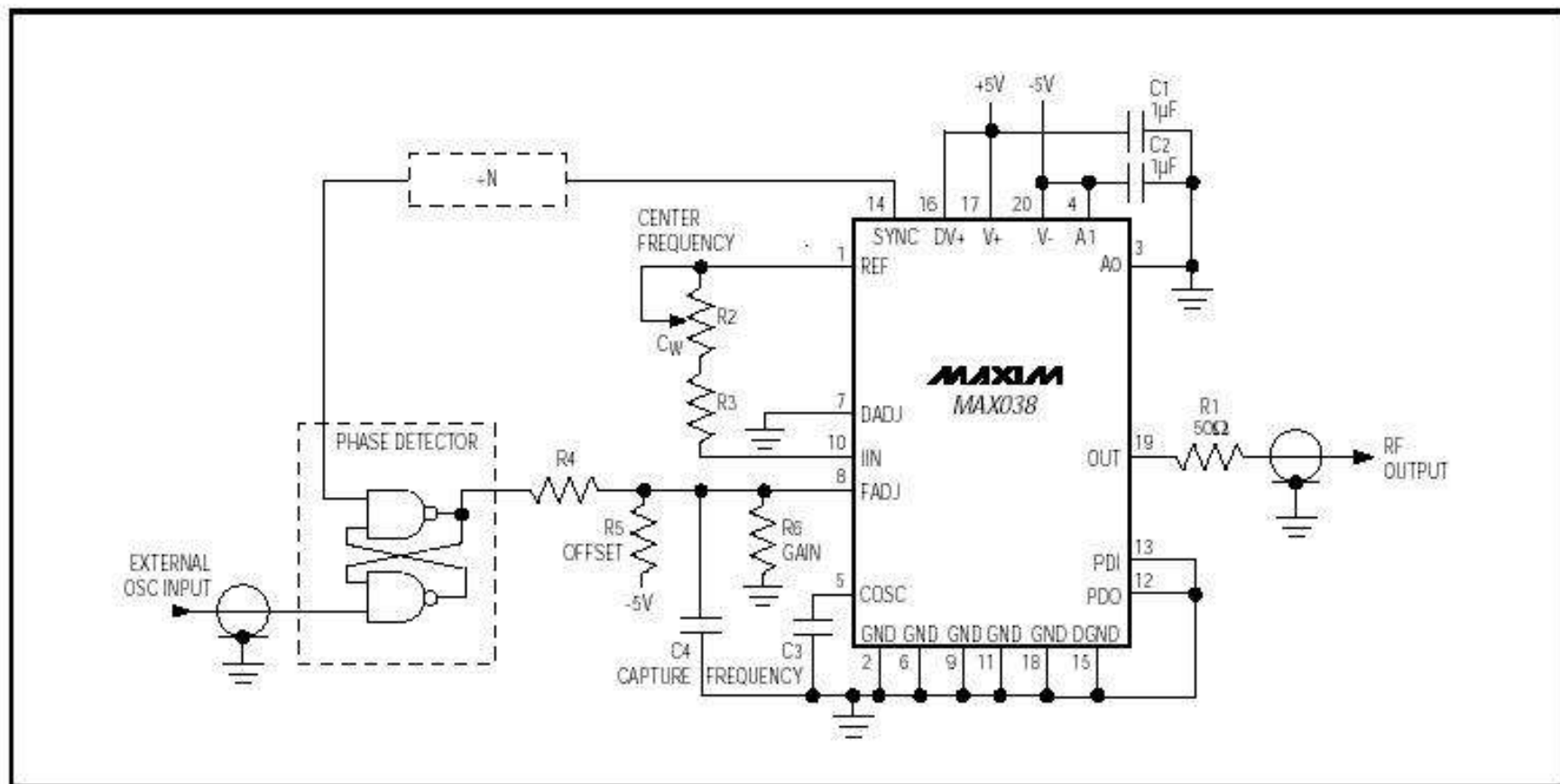


Figure 4. Phase-Locked Loop Using External Phase Detector

# Scalone odbiorniki radiowe

## TDA 7421N - SGS Thomson Microelectronics

**TDA 7421N** - AM/FM tuner for car radio and Hi-Fi applications.

Układ TDA 7421N jest scalonym, zintegrowanym odbiornikiem AM/FM przeznaczonym do stosowania w samochodowych odbiornikach radiowych oraz innych radioodbiornikach wymagających jakości dźwięku klasy Hi-Fi.

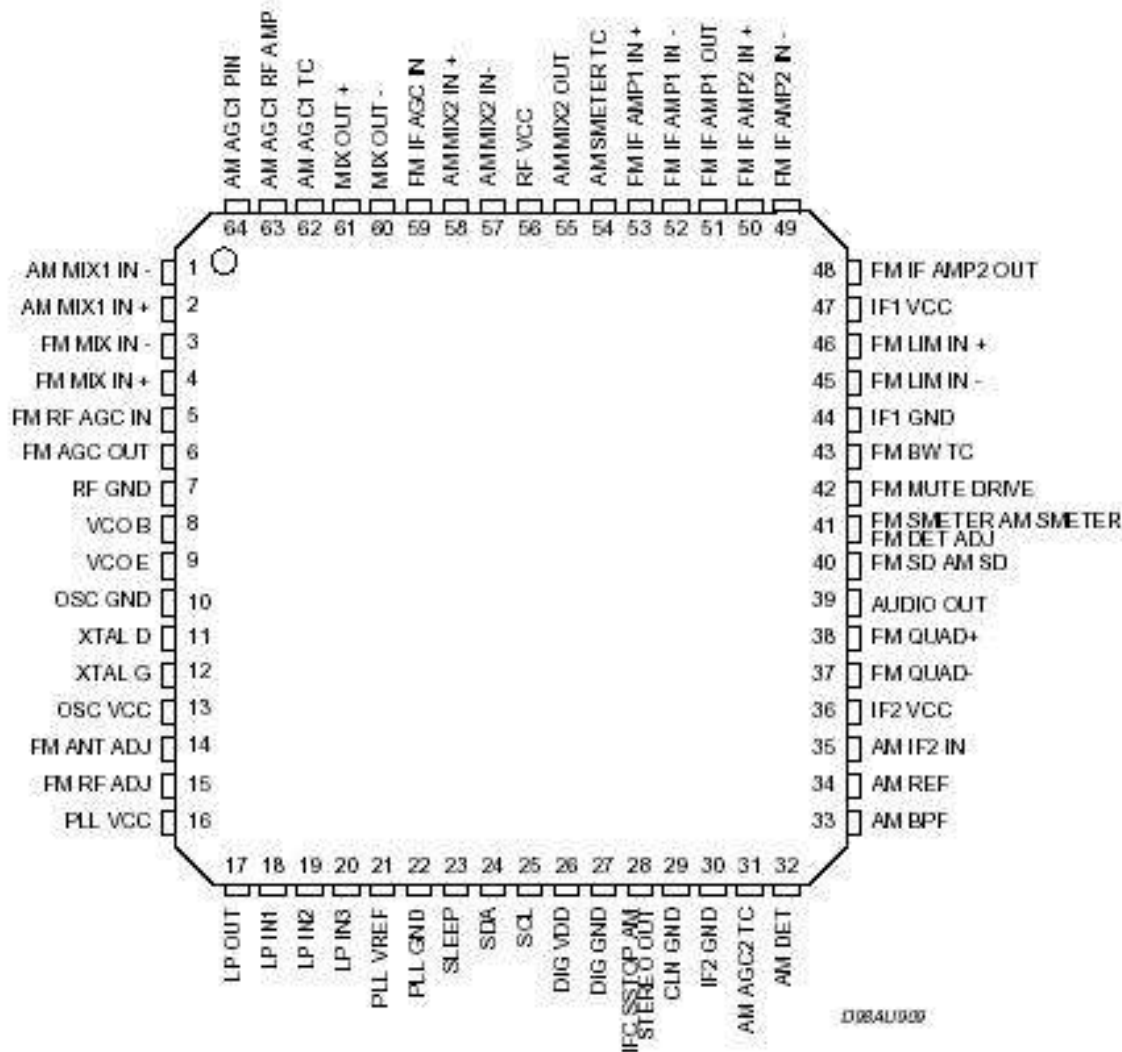
- HIGH PERFORMANCE FRONT-END IC FOR AM/FM RECEIVERS
- FULLY INTEGRATED HIGH-SPEED PLL FOR OPTIMIZED RDS APPLICATIONS
- FM MPX/AM AUDIO OUTPUT, 450kHz AM IF OUTPUT FOR STEREO AM APPLICATIONS
- AM DOUBLE CONVERSION ARCHITECTURE
- AM/FM STATION DETECTOR AND DIGITAL IF-COUNTER
- SINGLE FREQUENCY REFERENCE FOR BOTH AM AND FM
- FULL ELECTRICAL ADJUSTMENT
- I<sup>2</sup>C-BUS PROGRAMMABLE





# Scalone odbiorniki radiowe

## TDA 7421N - SGS Thomson Microelectronics

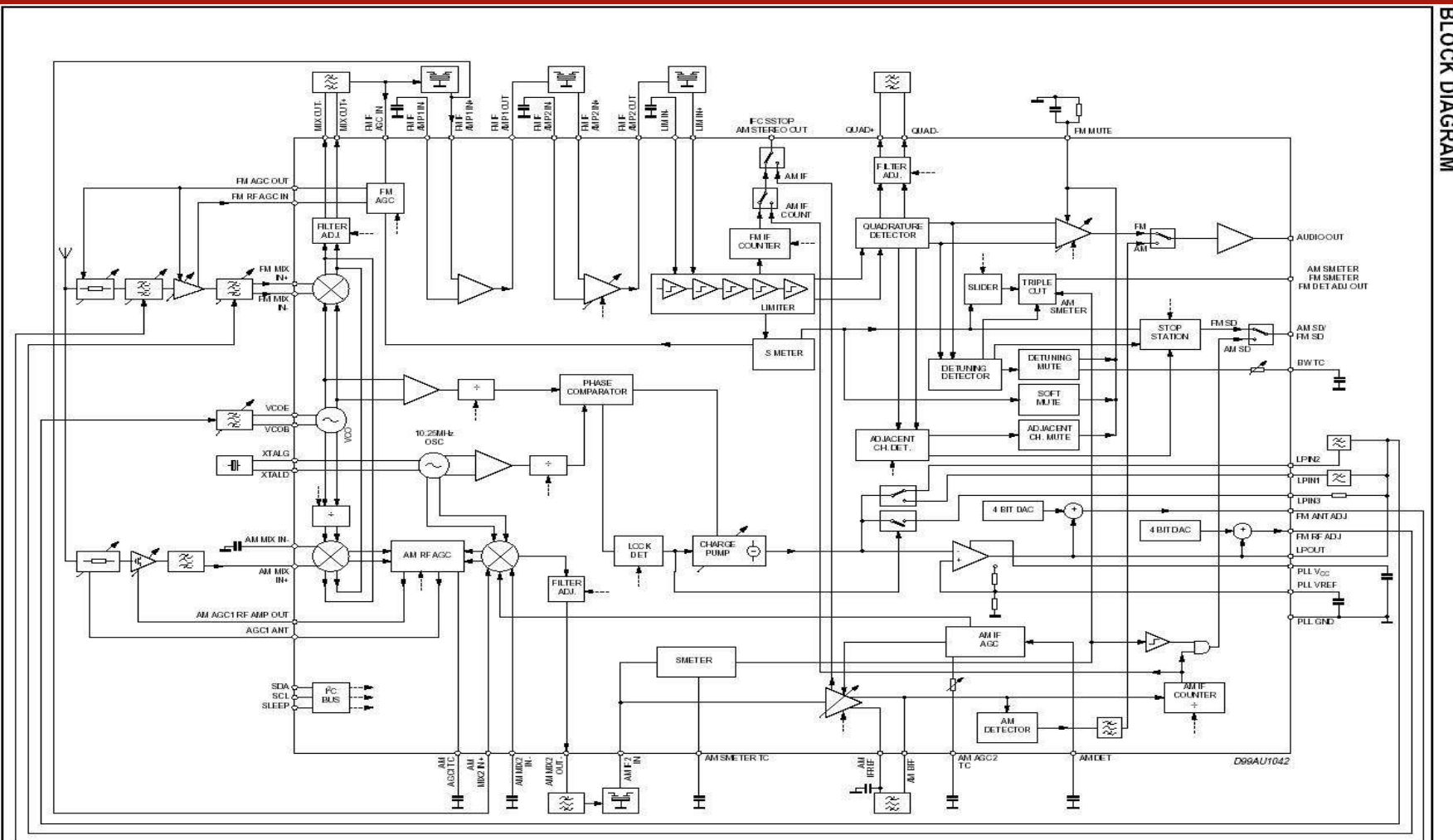






# Scalone odbiorniki radiowe

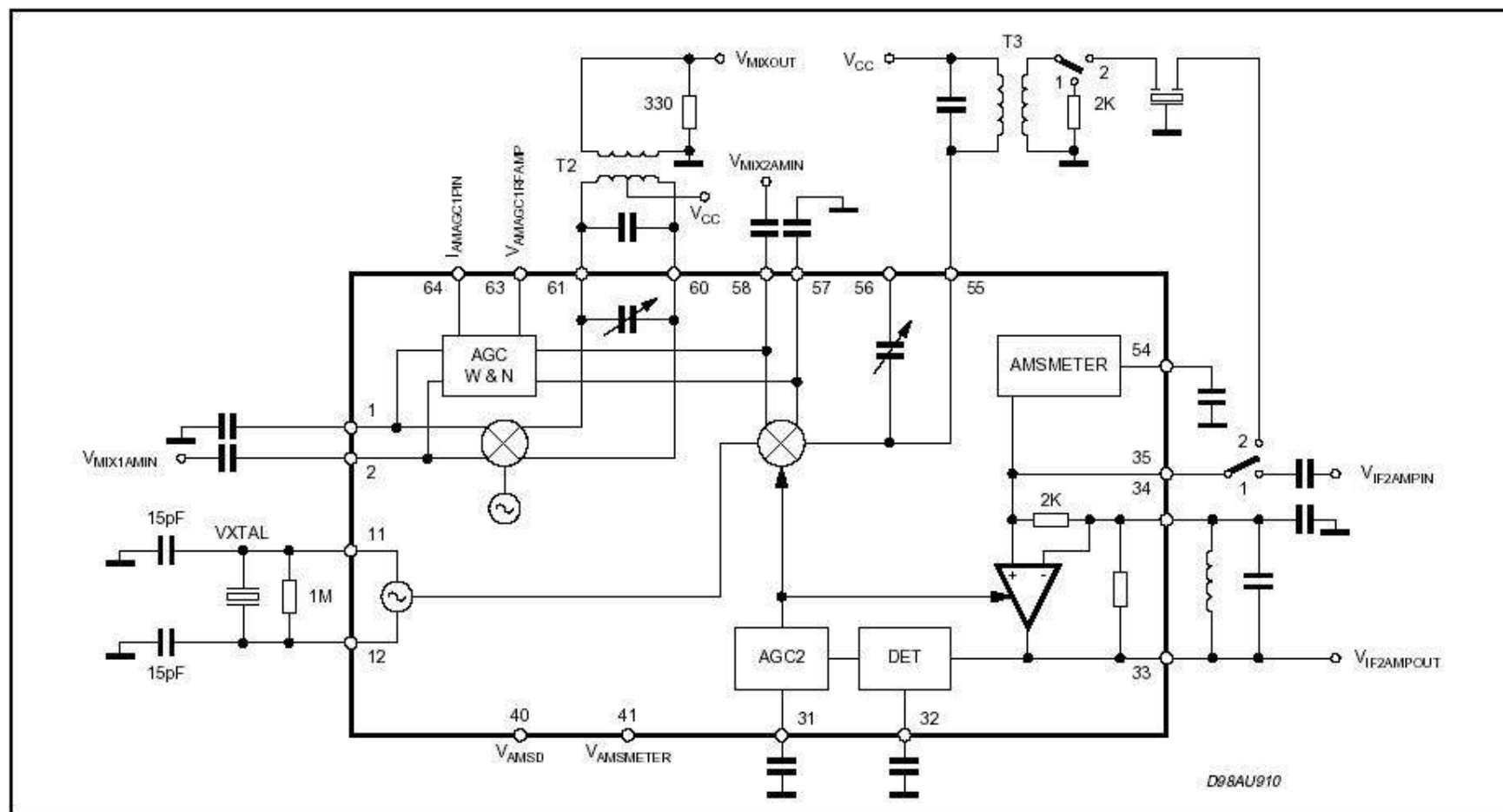
## TDA 7421N - SGS Thomson Microelectronics



# Scalone odbiorniki radiowe

## TDA 7421N - SGS Thomson Microelectronics

Figure 1. AM Test Circuit



# Scalone odbiorniki radiowe

## TDA 7421N - SGS Thomson Microelectronics

Figure 2. FM Test Circuit

